Development of Reduced Switch 21 Level Asymmetric Inverter without Inversion Circuit for Dynamic Load Conditions

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Abstract: Generating higher voltage steps at the load terminal using asymmetric configuration of DC source with limited switch count is more attracted by the researchers in recent days. Therefore producing higher voltage steps using multilevel inverter (MLI) with minimum part count leads to reduction in cost and size. So here a construction and software validation of a MLI to produce higher voltage level without inversion circuit is performed. The constructed MLI is able to provide 21 voltage steps at the load using 3 DC sources which are having unequal voltage values and 10 switches. The switching circuit is designed to perform the necessary logic pulse generation for the switches in the MLI circuit using nearest level scheme. Further software validation is done using MATLAB/Simulink and the designed MLI is tied to R, Z and induction motor loads and the THD% is observed as 4.73, 4.82 and 4.12 % . Also the inverter achieves a remarkable efficiency of 96.83% for a resistive load of 150Ω and 1000 W. This shows that the proposed MLI lowers THD which results in smoother operation of connected loads, reduced heating, and improved efficiency. The performance of the 21 voltage step MLI is observed and it is presented here. Also a comparison study based on switch count, independent source and THD% is made between the proposed MLI, conventional and recent MLIs. The hardware implementation is carried out using SPARTAN 6, and the results are presented for fixed and variable R and Z loads. Thus the proposed 21-level MLI stands out due to its; simplified topology with reduced component count, high-quality output waveform with low THD, broad applicability across load types, including dynamic motor loads and high efficiency with adherence to industry standards.

Keywords: Asymmetric inverter; modes of operation; multi-level inverter; power electronics; reduced switch component.

1. Introduction

Multi-Level Inverters (MLI) have become a revolution in the world of power electronics for its improved voltage and current waveforms, high power applications and for power quality demanding applications. They also find applications in speed drive control, STATCOMS, HVDC and HVAC transmissions. The advantages of multi-level inverters are used in higher voltage operability, reduced voltage derivatives, reduced voltage harmonic components, fault tolerant operation and increased efficiency. The current trend applications for MLIs are around photovoltaic conversions, electric vehicle technology, wind energy technology etc. MLI consists of various circuit components such as diodes, voltage sources and switches. Based on the construction of the circuit and the voltage sources considered, the inverters are classified as symmetric and asymmetric MLIs and to be specific they are further classified as: series-mode half-bridges, clamp-on diodes and capacitor-to-float converters [1]–[2].

In symmetric MLIs, the DC sources have the same amplitude in their configuration, whereas in asymmetrical inverters the sources have non identical source ratings in their configuration. All these types of conventional type MLIs have a greater number of switches in

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their design which directed to construct MLI with reduced components. As reduced number of switches is required, asymmetrical MLIs are identified for operation. Due to the reduced switch count, the switching power losses are lowered drastically. Also, another big advantage of asymmetrical configuration is that for the same switch count, higher level can be obtained in asymmetrical configuration compared to symmetrical configuration. Required parameters for the design of a MLI are number of levels to be acquired; count of the switches needed for the required levels, harmonic occupancy in voltage obtained at output, the count of independent DC sources needed to generate the required +levels, switch stress and the standing voltage.

However, for achieving more number of levels, greater quantities of switches are required. So, a solution is needed to have additional levels and to have reduced switching components [3]-[6]. For better performance of the MLI, the harmonic distortion finds a crucial role. The achievement of the MLI can be inferred from the amount of harmonic distortion present at the load current and voltage. The harmonic distortion must be reduced, so that the MLI performance can be improved. For the reduction of harmonic distortion, the PWM techniques engaged in the semiconductor switches plays a central role. This also helps in providing the required switching pattern such that a sinusoidal wave across the load can be achieved. In light of the aforementioned, numerous efforts have been made over the past few years to decrease the switch count; these efforts are covered in [7]–[11]. These works have produced some new topologies and structures with a smaller number, although each has flaws of its own.

Further, MLI configurations shown in [17] and [18] are capable of producing 13 levels at the load using 14 and 13 switches respectively. Where configuration developed in [17] uses capacitor for clamping the voltages and is of floating types but the number of DC sources present in [17] is 2 when compared to 4 in [18]. The presented MLI in [19] and [20] are able to give 17 levels at the load using 7 and 14 power switches. The MLI circuit in [19] and [20] needs extra capacitors, where the numbers of DC sources connected are 2 and 1. In [21], a 21 level inverter is experimented with 20 switches, 8 diode and capacitors each and 1 DC sources. So, in the view of considering the above discussion, to generate higher voltage levels, a new MLI is to be designed which involves minimum quantity of circuit components.

The proposed model is also a new topology structure with reduced switching component and taken into consideration of the shortcomings to produce a much higher level of output. The proposed model is a new topology for 21-level asymmetric MLI with only 10 switches and 3 unequal D.C. sources. The configuration does not possess inversion circuit, there by operability of the circuit is increased for higher range of voltages.

This paper follows through as given in section II describes the model of proposed circuit, the analysis of switch count, level count and the peak voltage followed by section III which provides the working, modes of operation and the switching sequence of the proposed circuit in a detail manner. Section IV is the results of the proposed model from the simulation. Finally in Section V, conclusions are made on the proposed model which gives a higher voltage with reduced switch count and reduced THD.

2. 21-level inverter with switching sequence

A MLI configuration [12] without inversion circuit is shown in Fig. 1. To obtain 21 levels, the proposed circuit consists of 10 switches and 3 voltage sources. Here, all 10 switches are uni-directional in nature as illustrated in Fig. 2, so that identical driver circuit is used for the switches present in the circuit. A basic sinusoidal PWM technique is used generating triggering pulses for the proposed model. The designed MLI circuit is formed with 3 unequal voltage sources which will make an asymmetric configuration. D.C. voltage sources are identified as 40V, 80V and 280V respectively.

A. MLI Design Criteria

For the inverter topology, mathematical equation is derived with the aim of finding the level count obtained from the inverter and switch count and the voltage sources required for the

inverter. Let the voltage sources required be switch count be N_{sw}, level count of the inverter be N_{lvl}.

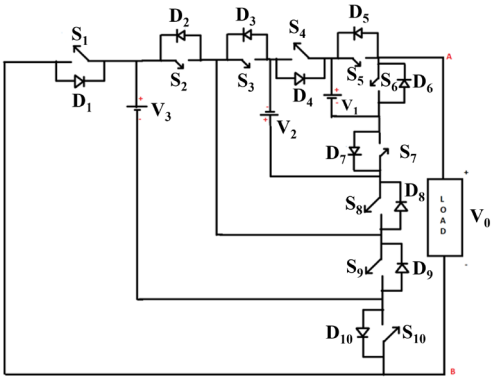


Figure 1. 21 Level Inverter

Figure 2. Switch Configuration

The switch count for the proposed inverter (N_{sw}) can be calculated as given in Equation 1,

$$N_{sw} = 2^m + 2 \quad (1)$$

The level count (N_{lvl}) for the figure 1 can be calculated from Equation2,

$$N_{lvl} = 7 \times m \quad (2)$$

The peak output voltage ($V_{0,\,max}$) of the inverter is achieved from Equation 3,

$$V_{0,\,max} = (2^m + 2) \times V_{DC} \quad (3)$$

Now the proposed topology consists of 3 voltage sources ($m = 3$), so switch count N_{sw}= 10, the level count of the inverter is N_{lvl} = 21. Here the $V_{DC} = V_1 = 40V$, so the peak output voltage can be given as $V_{0,\,max} = 400V$.

where '*m*' is the number of DC voltage sources and 'V_{DC}' is the fundamental DC voltage source value.

B. Pulse Generation

The pulses that are to be given to the switches are generated by using four divisions, sine wave signal as reference, comparator for comparing the reference wave and the gain, relational and logic circuit are used for producing the pulses for the switches and driver circuits for the triggering of the switches. These four divisions can be demonstrated as illustrated in Fig. 3.

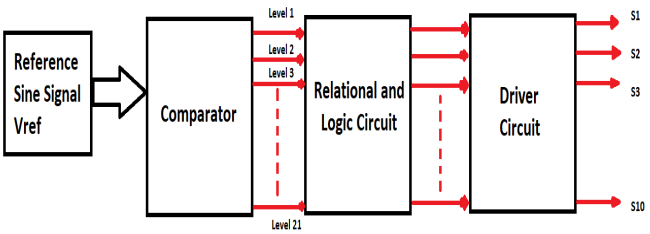


Figure 3. Various Divisions of Pulse Generation

From the block diagram (Fig 3), a sine wave is taken as reference and the amplitude of the reference wave is taken as 11V. Its chosen based on the positive level and zero level needed for the MLI. This reference wave is given as the input to the comparator. The output of the comparator obtained is directed to relational and logic circuit block. Here relational operators

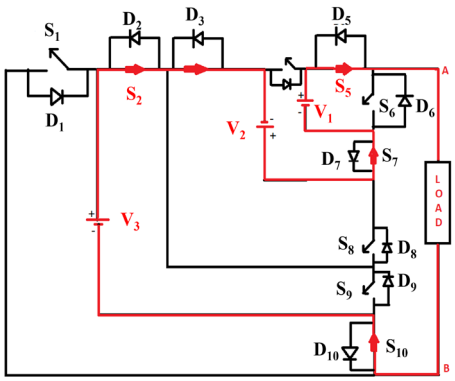
are used to compare the levels that are to be selected. For each level a pair of relational operators and an AND gate is used for the generation of the pulses. This output is sent to a driver circuit which consists of a sum block and multiport switch block. The sum block collects all the pulses that is to be selected for each switching sequence. The switching order in which the switches are to be switched on is provided by the multiport block. The switching sequence of the appropriate level is coded into the multiport block as its input for each level. Right now the four divisions are implemented for each level coded with their respective switching sequence and then given to the IGBT switches used in the proposed configuration.

C. Modes of operation

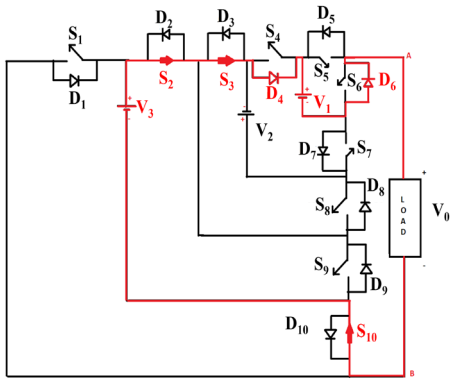
The inverter is designed to work in 21 modes of operation to construct an alternating waveform. For understanding purpose; few modes are explained in Fig. 3. Device status for each mode of operation is given below,

Mode-1:S_2, S_3, S_5, S_7, S_{10} devices are 'ON' to generate 400V
Mode-2: S_2, S_3, S_6, S_7, S_{10} devices are 'ON' to generate 360V
Mode-3: S_2, S_5, S_7, S_8, S_{10} devices are 'ON' to generate 320V
Mode-4: S_2, S_3, S_4, S_5, S_{10} devices are 'ON' to generate 280V
Mode-5:S_2, S_3, S_4, S_6, S_{10} devices are 'ON' to generate 240V
Mode-6:S_1, S_3, S_6, S_7, S_9 devices are 'ON' to generate 200V
Mode-7:S_2, S_4, S_6, S_8, S_{10} devices are 'ON' to generate 160V
Mode-8:S_3, S_5, S_7, S_9, S_{10} devices are 'ON' to generate 120V
Mode-9:S_9, S_6, S_7, S_9, S_{10} devices are 'ON' to generate 80V
Mode-10:S_5, S_7, S_8, S_9, S_{10} devices are 'ON' to generate 40V
Mode-11:S_6, S_7, S_8, S_9, S_{10} devices are 'ON' to generate 0V
Mode-12:S_3, S_4, S_6, S_9, S_{10} devices are 'ON' to generate -40V
Mode-13:S_4, S_5, S_8, S_9, S_{10} devices are 'ON' to generate -80V
Mode-14:S_4, S_6, S_8, S_9, S_{10} devices are 'ON' to generate -120V
Mode-15:S_1, S_3, S_5, S_7, S_9 devices are 'ON' to generate -160V
Mode-16:S_1, S_3, S_6, S_7, S_9 devices are 'ON' to generate -200V
Mode-17:S_1, S_5, S_7, S_8, S_9 devices are 'ON' to generate -240V
Mode-18:S_1, S_6, S_7, S_8, S_9 devices are 'ON' to generate -280V
Mode-19:S_1, S_3, S_4, S_6, S_9 devices are 'ON' to generate -320V
Mode-20:S_1, S_4, S_5, S_8, S_9 devices are 'ON' to generate -360V
Mode-21:S_1, S_4, S_6, S_8, S_9 devices are 'ON' to generate -400V

From the modes of operation, the Fig. 4 is drawn to demonstrate the switching states of the inverter circuit.



(a)


S1
D2
D3
S4
D5
D1
S2
S3
D4
S5
S6
D6
V3
V1
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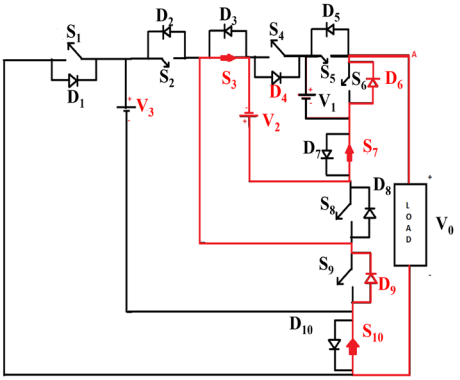
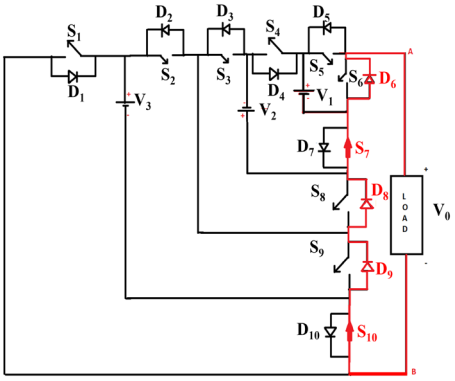
D7
S7
D8
S8
LOAD
V0
S9
D9
D10
S10
A
B

(b)


S1
D2
D3
S4
D5
D1
S2
S3
D4
S5
S6
D6
V3
V1
V2
D7
S7
D8
S8
LOAD
V0
S9
D9
D10
S10
A
B

(c)


S1
D2
D3
S4
D5
D1
S2
S3
D4
S5
S6
D6
V3
V1
V2
D7
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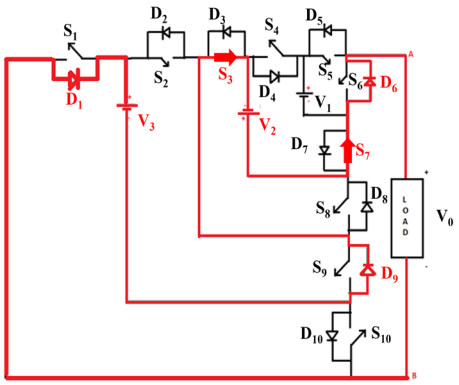
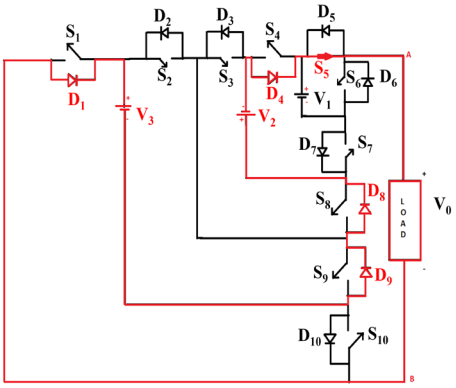
D8
S8
LOAD
V0
S9
D9
D10
S10
A
B

(d)



(e)

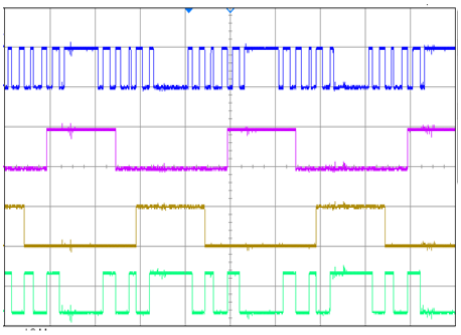


(f)

Figure 4. Modes of Operation for 21 level inverters

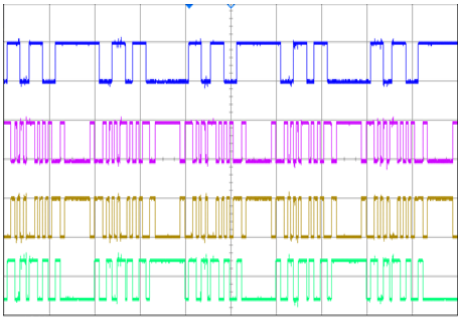
3. Simulation and Results

The Fig 5a to 5c shows the PWM pulse generation waveforms to the inverter circuit. In Fig. 5d, the simulated result of the proposed inverter simulated in MATLAB/SIMULINK with resistive load of 150Ω is shown.THD of the inverter's voltage wave shape is 4.73% and it is inside the scope of guidelines as given in IEEE 519. The proposed circuit constructs a crest-to-crest voltage of ±400V as illustrated from Fig. 4.



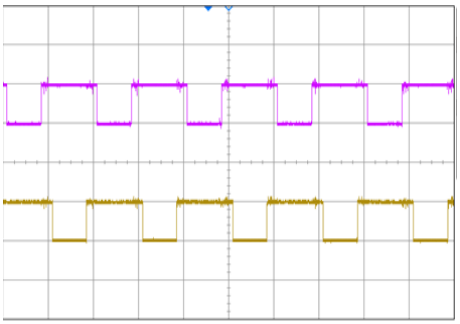
X axis - 1 cm = 0.01 seconds
Y axis - 1 cm = 1 volt

Figure 5(a). Input pulses generated for switches S_1 to S_4



X axis - 1 cm = 0.01 seconds
Y axis - 1 cm = 1 volt

Figure 5(b). Input pulses generated for switches S_5 to S_8



X axis - 1 cm = 0.01 seconds
Y axis - 1 cm = 1 volt

Figure 5(c). Input pulses generated for switches S_9 and S_{10}

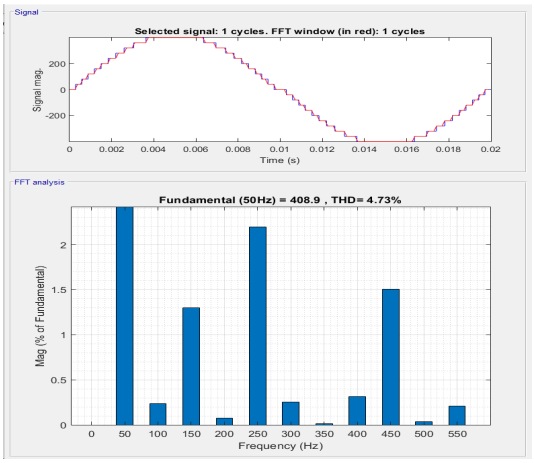


Figure 5 (d). Results of the circuit tied with R Load of 21-level inverter (Voltage THD)

Further, the proposed circuit is simulated for a R-L load, with R=150 Ω, L = 0.477 H. The output voltage for the RL load for the proposed inverter is displayed in Fig. 5e and the THD for the presented inverter's output voltage is 4.82% and current THD is 2.78% as shown in Fig. 5f.

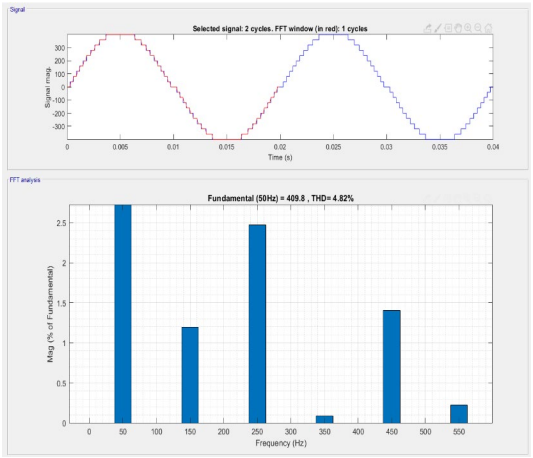


Figure 5(e). Results of the circuit tied with RL Load of 21-level inverter (Voltage THD)

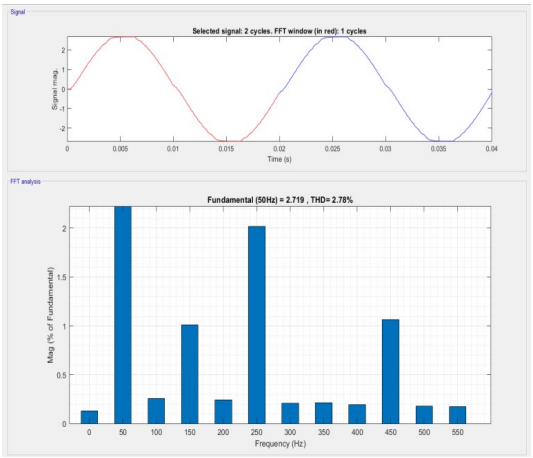


Figure 5(f). Results of the MLI circuit tied with RL load (Current THD)

Calculation of Power loss for proposed Multi level Inverter

The primary cause of the conduction loss (P_{cl}) in power semiconductor switches are dues to its internal resistance R_{in} during their on-state and P_{cl} can be computed using equation 4,

$$P_{cl}= \sum_{j=1}^{14} R_{in}\, I_{Out}{}^{2} \quad (4)$$

Turn-on power loss ($P_{swl,ON}$) and turn-off power loss ($P_{swl,OFF}$) are the terms which describes the switching losses that results from the overlap of current and voltage across the switches during the transition of switching states and it is computed from 5 to 8.

$$P_{swl,ON}= fs \int_0^{t_{on}} v(t)i(t)dt = fs\left(\frac{-Vb(t-t_{on})}{t_{on}}\right)\left(\frac{I_{out}}{t_{on}}t\right)dt = \frac{1}{6} fs\, V_{bl} I_{out} t_{on} \quad (5)$$

$$P_{swl,OFF}= fs \int_0^{t_{off}} v(t)i(t)dt = fs\left(\frac{-Vb(t-t_{off})}{t_{on}}\right)\left(\frac{I_{out}}{t_{off}}t\right)dt \quad (6)$$

$$P_{swl}=P_{swl,ON}+P_{swl,OFF} \quad (7)$$

$$P_{swl}= \sum_{j=1}^{14} fsj * Vbj * Iout * (ton + toff) \quad (8)$$

The total power losses (P_{pl}) and the efficiency are obtained as

$$P_{pl} = P_{cl} + P_{swl} \tag{9}$$

$$\eta = \frac{P_o}{P_o + P_{pl}}$$

[(P_o) is obtained from V_{rms}*I_{rms}] (10)

From the above equations the efficiency of the proposed 21 level MLI is obtained as 96.83% for 150 Ω, 1000 W load. The proposed circuit is also simulated for induction motor load with specification as provided in Table 1 and Fig. 5g shows the main winding current of the induction motor tied with 21-level inverter.

Table 1. Specification of IM load

S.No.	Parameter	Values
1.	Power rating	0.25 HP
2.	Rated speed	1440 RPM
3.	Number of poles	4
4.	Voltage Rating	230 V
5.	Current Rating	4.8 A
6.	Rated Torque	2.2 Nm
7.	Frequency	50 Hz

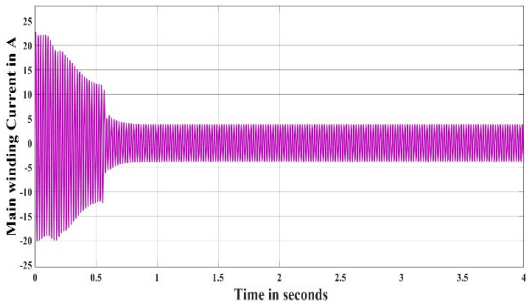


Figure 5(g). Results of the 21-level circuit tied with induction motor load (main winding current)

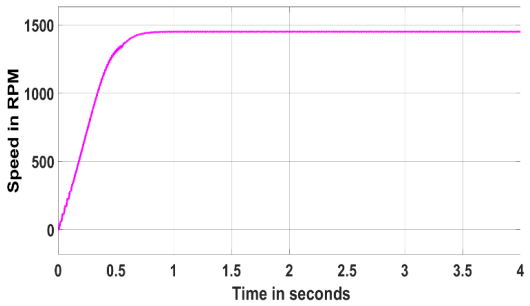


Figure 5(h). Results of the MLI circuit tied with induction motor load (Speed)

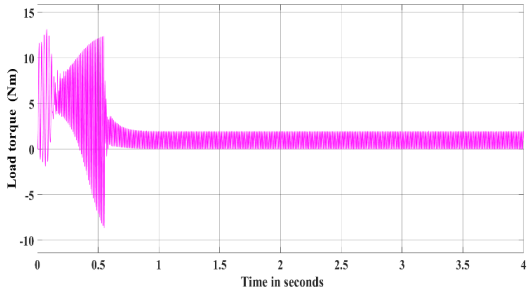


Figure 5(i). Results of the inverter circuit tied with induction motor load (Load torque)

When the circuit is tied with an induction motor, the motor settles at a speed of 1451 rpm, due to a load torque of 2 Nm, as presented in Fig. 5h and 5i respectively. Now the THD of the circuit after connecting it with a motor load is 4.12% that can be shown in Fig. 5j.

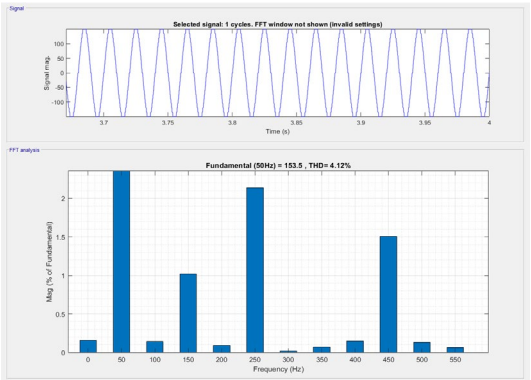


Figure 5(j). Results of the circuit tied with induction motor Load of 21-level inverter (Voltage THD)

4. Comparative Study

Multiple structures for the MLI have been presented to reduce the switch count. The structure realized in [13] is a 51-level symmetric structure consisting of 9 level structures in cascade with an H-bridge circuit. This structure has 25 independent sources, each having a magnitude of 1 Volt, along with 46 power switches. Due to the symmetrical structure, achieved output voltage is less, but the circuit has a low THD value of 1.95%. The proposed MLI in [14] produced 31-levels are obtained using asymmetric configuration. This configuration consists of ten power switches and six independent sources. The negative levels obtained using an H-bridge and the THD value obtained for reactive load is 3.18%. By using the basic principle of CHB inverters, a new cascaded topology is realized in [15]. The basic unit is made of 3 independent sources and 5 power switches. This basic unit is cascaded with H-bridge to obtain multiple levels. Using one base unit 9 levels are achieved with a THD value of 18.8%. Cascading two basic units, a 15 level inverter is achieved with a THD value of 14.16%. By cascading the basic unit the output voltage levels that are obtained are 27, 33, 39 and their respective THD values are 12.07, 11.85 and 11.33% respectively. In [16] 57-level inverter is realized which is constructed using 9 cascaded structures with an H-bridge. The basic unit consists of 3 independent sources and 6 power switches. The symmetric configuration consists of a total switch count of 51 and 28 independent sources to obtain the 57-level output. Also, the same levels of output can be obtained in an asymmetrical configuration with only two basic units where the switch count is 18 and the number of independent sources is seven.

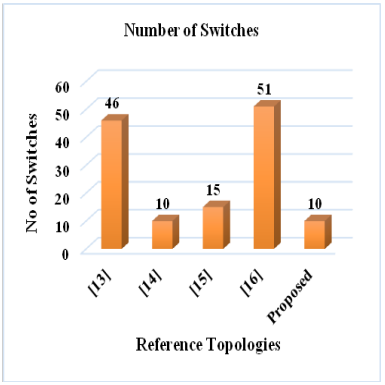


Figure 6(a). Comparative study for switch count

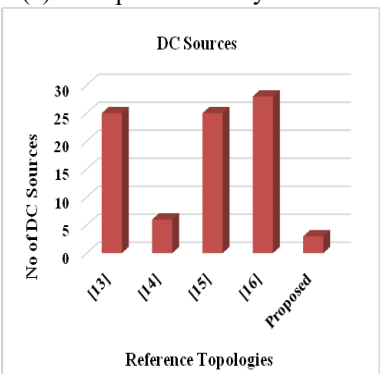


Figure 6(b). Comparative study for independent sources

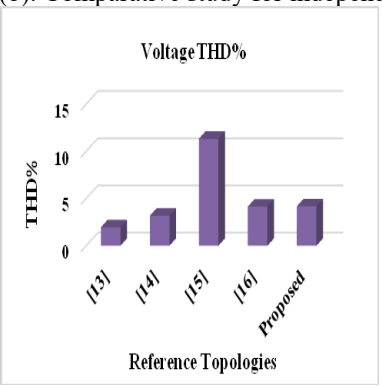


Figure 6(c). Comparative study for THD%

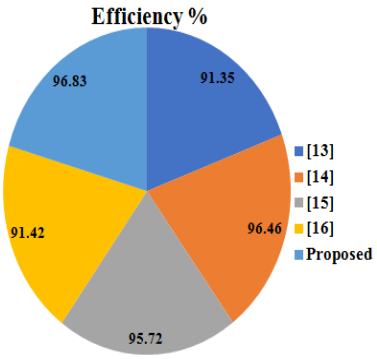


Figure 6(d). Comparative study for efficiency%

Also analysis is made for the efficiency of the proposed inverter with other MLI's for the same power and it is calculated as 96.83%. Comparative plot on switch count, independent source, THD% and efficiency for the reference papers [13] – [16] with respective to proposed topology is exhibited in Fig. 6(a), 6(b), 6(c), and 6(d) respectively. A 21-level configuration of MLI which make use of minimal switch count has been designed and the proposed circuit can achieve the maximum voltage with minimum number of switches with a low THD, thereby reducing the cost and size. Comparison between the proposed circuit with traditional inverters such as: cascaded H-Bridge, diode clamped and flying capacitor inverters are demonstrated from Fig. 7 (a) to Fig 7 (e).

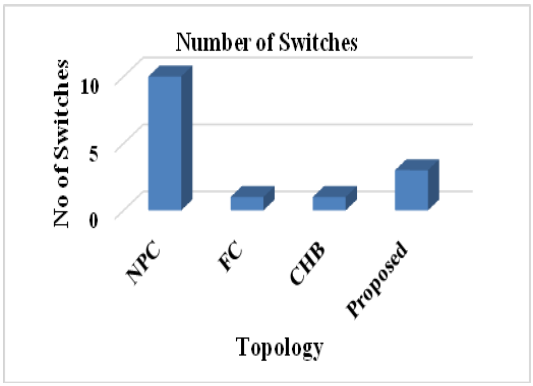


Figure 7(a). Number of Switches

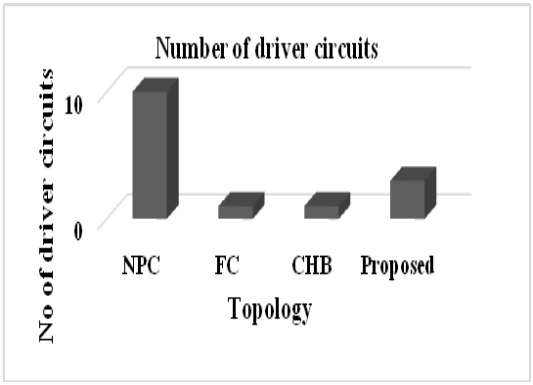


Figure 7(b). Number of driver circuits

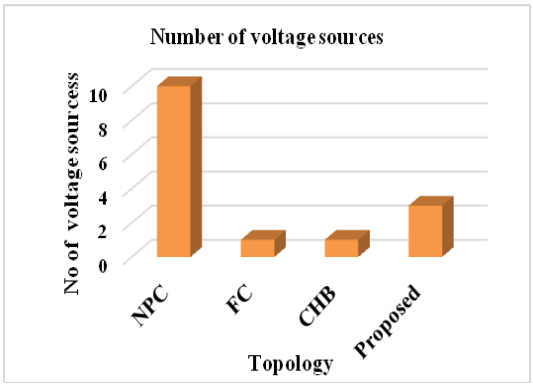


Figure 7(c). Number of voltage sources

5. Real time validation

From the comparative study it is proved that design of 21-level inverter discussed here utilizes minimum number of components compared to the other MLI designs. Therefore the hardware implementation of the 21-level multilevel inverter is carried out with the components as given in Table 2. It involves the various parts like the power supply, inverter circuit, FPGA controller unit and the driver circuit. Using VHDL coding, program is written and dumped into the FPGA SPARTAN 6 controller unit and using driver circuit the pulses will be given to the IGBT's that are present in the 21-level MLI. Finally, the performance of the inverter is studied by connecting it to fixed R and Z load, variable R and Z load conditions.

Table 2. Components of hardware implementation

S.No.	Components	Specifications
1.	IGBT	15N120NDS
2.	Driver Circuit	TLP250_DR
3.	Controller	FPGA SPARTAN 6
4.	Inductance load	120 mH
5.	Rheostat	100 Ω, 2 A
6.	Capacitor	680 µF

The magnitudes of the DC sources are selected as: V_1 = 40 V, V_2 = 80 V, V_3 = 280 V for the real time implementation. For validation of the proposed inverter, a prototype of multilevel inverter circuit is developed and tested as shown in Fig. 8.

A. 21-Level MLI with Resistive Load

The hardware setup is shown in Fig. 8 is connected to a resistive load of R=100 Ω and the output voltage, current is viewed from DSO. Fig. 9 shows both the current and voltage waveform at the output. This depicts that, both the voltage and current waveform are in phase with each other. The output voltage has the maximum value of ±400 V and the output current value of 0.4 A.

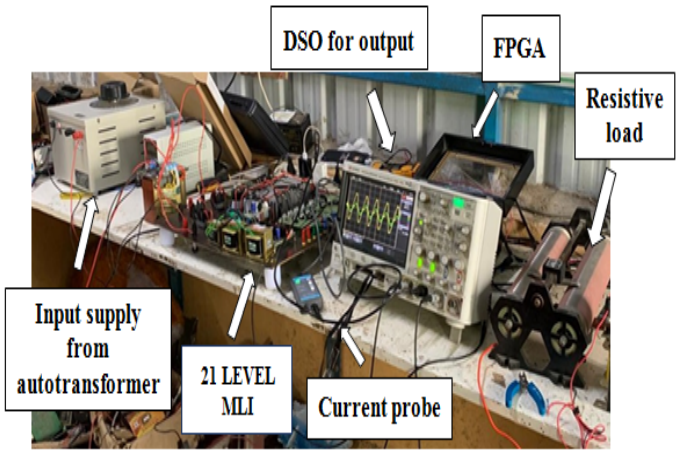


Figure 8. Hardware implementation of 21-level MLI for resistive load

To check the stability of the inverter, it is tied to variable R load conditions (ie., the resistance value is being varied from a low value to certain high value) and the performance of the inverter is observed satisfactory. Fig. 10 depicts the output voltage and current waveform for variable R load conditions. The current waveform (2) clearly shows the variation of the current while the resistance is being varied. The current value is larger while the resistance value is low and decreases furthermore while the resistance value is lowered.

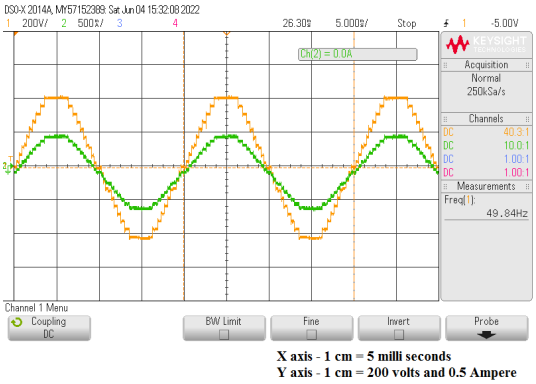


Figure 9. 21-level MLI output voltage and current waveform for resistive load

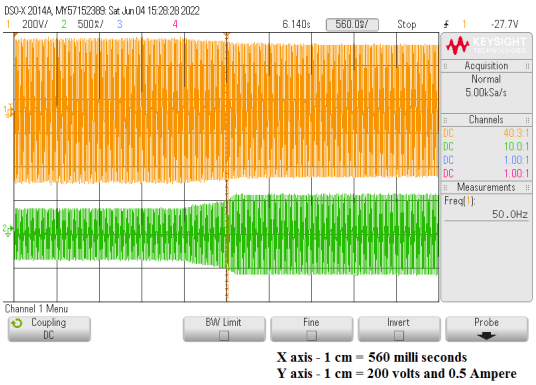


Figure 10. 21-level MLI output voltage and current waveform for variable R load

B. 21-Level MLI with Reactive Load

The hardware setup for the 21-level MLI for reactive load is shown in Fig. 11. The resistance value is kept at R=100 Ω and inductance L=120 mH.

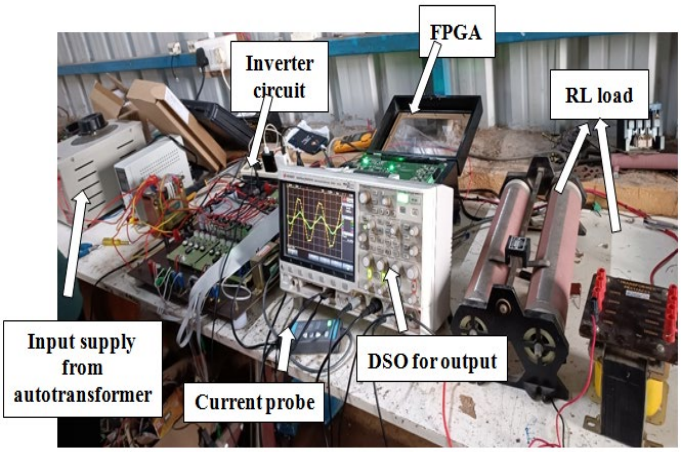


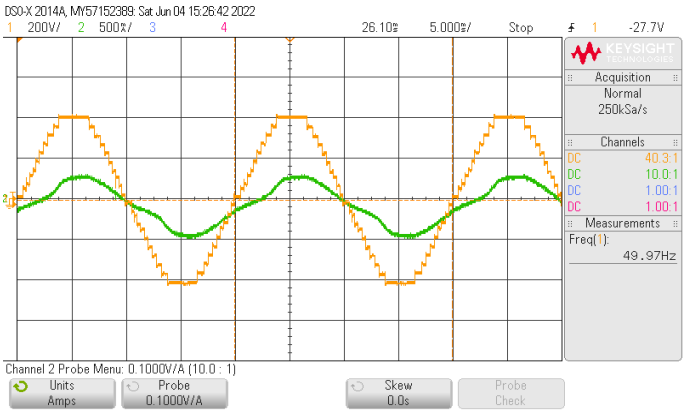
Figure 11. Hardware implementation of 21-level MLI for RL load

Fig. 12 depicts the output voltage waveform and current waveform and the load values are observed as ±400 V and 0.3 A respectively. From the load waveform, it is seen that the current waveform clearly indicates that in inductive load condition the current lags the voltage. The

comparison for the THD at the output voltage for both the simulation and hardware results are represented in the Table 3 and it is seen that the observed values are as per the IEEE standard.

Table 3. THD comparison of 21-level MLI

S.No.	21 – level MLI with	THD (OUTPUT VOLTAGE)	
		Simulation results	Hardware results
1.	R load	4.73 %	4.86 %
2.	RL load	4.82%	4.93 %



X axis - 1 cm = 5 milli seconds
Y axis - 1 cm = 200 volts and 0.5 Ampere

Figure 12. 21-level MLI output voltage and current waveform for RL load

The inductance value is maintained constant at L=120 mH but the resistance value is being varied. Fig. 13 depicts the output voltage waveform and current waveform for variable RL load. The current waveform in Fig. 13 clearly shows the variation of the current while the resistance is being varied. The current is larger while the resistance value is low and decreases furthermore while the resistance value is lowered.

X axis - 1 cm = 560 milli seconds
Y axis - 1 cm = 200 volts and 0.5 Ampere

Figure 13. 21-level MLI output voltage and current waveform for variable RL load

6. Conclusion

As the inverter plays a vital role in renewable energy integration, here a 21 level inverter is designed using 3 DC asymmetric voltage sources, 10 power switches. A thorough analysis is made to design the 21-level MLI. Further, the proposed circuit is drive through fundamental frequency pulse width modulation and it is modeled in MATLAB/Simulink environment and the simulation results are presented. The design parameters are compared with conventional MLI, recent MLIs and it is inferred that the proposed 21-level MLI performs better compared than the other MLI designs. In continuation with this, the hardware implementation is carried and satisfactory results have been obtained. The simulation results showing THD values of 4.73% for resistive loads and 4.82% for RL loads. Hardware implementation results closely align with these values (4.86% and 4.93%, respectively), validating the design and meeting IEEE 519 standards. Also while connected to an induction motor load, the MLI provided efficient performance with low THD (4.12%). The motor achieved stable operation at 1451 RPM under a load torque of 2 Nm, confirming the inverter's suitability for motor drive applications. The hardware implementation further validates the design, demonstrating excellent agreement between simulation and real-time results. Stability and reliability are confirmed under both fixed and variable load conditions. The presented work can be extended to integration of renewable energy sources such as solar PV or fuel cells. Thus the proposed 21-level MLI achieves high-quality performance with reduced hardware requirements, making it a promising solution for modern power electronics applications.

7. Acknowledgment

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