High Voltage Gain Non isolated DC-DC Converter based on MSIC- MBM for Photovoltaic system

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Abstract: This paper proposes a High Voltage Gain DC-DC converter for Renewable Energy Systems (RES) based on a Modified Switched-Inductor Capacitor (MSIC) to achieve high voltage gain for photovoltaic systems. Additionally, the Modified Boosting Mode (MBM) is combined with the MSIC to further enhance voltage gain. The MSIC employs a diode in series with the inductor to achieve high voltage gain and prevent pulsating input current at low duty cycles. Furthermore, the MSIC is interleaved with the main switch to manage current when the system supplies high load current. Moreover, the MBM is incorporated into the proposed converter with an auxiliary switch to verify high voltage gain using Zero Current Switching (ZCS) across the auxiliary switch. This approach helps reduce conduction losses when the system supplies high load currents. The diodes in the MSIC and MBM operate under low current and voltage stress when the system supplies high load currents, thereby reducing the stress on the power devices at high voltage gain and decreasing the overall power loss of the system. The converter utilizes high switching frequencies to achieve high efficiency, low passive component values, reduced switching and conduction losses, a compact size, and decreased circuit weight. The paper investigates the steady-state analysis and mathematical model of the converter, considering two operational modes: Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). The efficiency of the proposed converter has been analyzed, and the operation has been verified using MATLAB Simulink. In addition, the proposed converter achieves higher voltage gain with lower voltage stress across components compared to previous DC-DC converters. Additionally, a 200W PCB prototype design has been implemented to validate the experimental results.

Keywords: Non isolated DC-DC Converter, MBM, MSIC, ZCS.

1. Introduction

Renewable energy systems like solar and wind power are essential for addressing global energy challenges by providing clean and sustainable electricity [1, 2]. Advanced power electronics are needed to manage this energy, adapt voltage levels, and integrate with the power grid. High voltage gain DC-DC converters are crucial for efficiently transferring power from renewable sources to the grid or storage systems [3, 4]. SEPIC and boost converters are commonly used in applications such as electric cars, photovoltaic systems, motor drives, LED drivers, aerospace, fuel cells, and electric aircraft [5, 6]. However, these systems often require high DC voltages, which low-voltage sources like photovoltaic panels and fuel cells cannot directly provide [4, 30]. Connecting multiple panels in series to achieve high voltage can be inefficient and expensive.

To address this challenge, DC-DC converters are used to boost low input voltages to high output levels, either fixed or variable, to meet application-specific requirements. These converters achieve significant voltage gain but face issues like high voltage stress on diodes and MOSFETs, as well as efficiency loss due to parasitic resistance in capacitors and inductors[7,8]. The number of passive components also impacts voltage gain. For instance, while a boost converter can achieve high gain with a high duty ratio, it suffers from reduced efficiency and increased current stress on components. Zeta converters, often used for voltage stepping, face issues like fluctuating input current and high voltage stress on switches. Traditional boost converters avoid input current pulsation due to a series inductor, enabling higher efficiency, but they face challenges at low duty cycles, such as input current dropping to zero[9,10]. This

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requires larger inductance, leading to higher resistance, lower efficiency, increased costs, and poorer performance. To mitigate input current pulsation at low duty cycles, this paper proposes adding a diode in series with the inductor[11].

Many research has gone into the development of DC-DC converters with modifications to the boost, buck-boost, non-coupled inductor SEPIC, and converters utilizing coupled inductors, aiming to secure high voltage gains for a plethora of applications. However, these designs often encounter limitations due to the extensive use of passive components, lower switching frequencies, and the need for larger inductors and capacitors, which elevate the stress on the system's power diodes and switches. Additionally, these designs can suffer from zero input current at low duty cycles. A specific non-isolated boost DC-DC converter model was initially introduced and later refined to attain higher voltage gain. Nonetheless, its efficiency is compromised due to the dual path of the input current during the 'on' state and the pulsation of inductor current at low duty cycles, rendering it less effective for RES. Moreover, the voltage gain is significantly impacted when employing a large number of components, thereby affecting the system's power density. Several converter topologies have been devised to achieve high voltage gains, employing conventional SEPIC converters with coupling inductors, three-phase DCM isolated DC-DC SEPIC converters, flyback converters with transformers, and double CUK converters interleaved for power factor correction (PFC). However, these designs often grapple with the issue of high leakage current due to the coupled inductor, potentially leading to voltage spikes through the parasitic capacitance of the MOSFET switches. Addressing the leakage inductance issue, clamping capacitors have been added to the switches in several designs. Yet, the introduction of more components tends to increase the parasitic elements, thereby diminishing the overall system efficiency. Several DC-DC converters have been proposed, such as using switching capacitors with diodes (SC) in [4, 14, 15] and switching inductors in [20]. In addition, another topology is introduced in [21], which achieves high gain ratio using only 10 switches and three capacitors. However, these topologies require more switches, making the gate drive circuit complex to build and implement. Research has been conducted on adapting traditional SEPIC converters to attain a high voltage gain, as noted in [3, 11, 13-24]. However, these converters have the drawback of power switches experiencing high voltage and current stress. Furthermore, to attain the desired voltage gain ratio, a lower switching frequency is utilized. The high on-resistance of power switches, combined with large inductors and capacitors that have significant internal resistance, presents challenges.

Some researchers have developed non-isolated DC-DC converters to step up low input voltages to high output voltages. However, these converters require very high duty cycles, necessitating a large number of inductors with high values and low switching frequencies. Using silicon (Si) MOSFETs instead of silicon carbide (SiC) MOSFETs reduces output voltage gain and increases switching losses. Other converters proposed in [9, 16, 25] include a four-level buck-boost DC-DC converter based on soft switching, a new bidirectional DC-DC converter based on ZCS, and cascaded converters for achieving high voltage gain. While these converters do achieve high gain, they also depend on high duty ratios and require many active components in [16-29] and passive and active elements in [9] to reach high gain ratios. However, the switches in these converters require complex gate drive control circuits, resulting in complicated, heavy, large, and costly systems [31, 32]. Additionally, at low duty cycles, the input current approaches zero, making these converters unsuitable for renewable energy systems (RES) due to their reliance on many high-value inductors at low switching frequencies.

This study introduces enhanced DC-DC converters designed for renewable energy systems, employing a novel method that integrates MSIC and MBM to achieve superior voltage gain. The innovation involves placing diode D_1 in series with inductor L_2, as shown in Figure 1, enabling the converter to achieve a stable input current at minimal duty cycles. Through the resonant operation of L_2 with the associated capacitor C_1, D_1 operates at ZCS, thereby reducing the voltage stress on power MOSFETs and diodes. Furthermore, the inclusion of MBM allows the power MOSFET to experience less voltage stress while achieving high voltage gain, which in turn reduces switching losses. The integration of the MSIC significantly reduces current and voltage

stresses on the primary power MOSFET switch and diodes. By adopting a higher switching frequency, the converter enhances efficiency and minimizes the size of circuit components, resulting in a lighter design. Additionally, the use of Wide Band Gap (WBG) power devices, characterized by low on-state resistance (Ron) at elevated switching frequencies, further amplifies voltage gain. This proposed converter design, which does not employ transformers or coupled inductors for voltage isolation between the input and output, offers advantages in terms of weight and compactness over previous models. It is capable of elevating a low input voltage ranging from 20 to 40 V to an output of 200 V at 200 W, with a duty cycle of 42%.

2. Operation and Structure of the Proposed Converter

The proposed DC-DC converter design introduces a modified structure that combines a Modified Switched-Inductor Converter (MSIC) and Modified Boosting Technique (MBT), incorporating a diode in series with the inductor and capacitor to achieve high voltage gain for renewable energy systems RES. As illustrated in Figure 1, this converter comprises three inductors, four capacitors, four diodes, and two power MOSFETs. This design provides multiple advantages, such as a steady input current without pulsation at low duty cycles and minimized voltage pressure on the Q_{S1} and Q_{S2} switches. This contributes to greater flexibility in modifying duty cycles and supports the handling of higher load currents. Additionally, the converter's efficiency is exceptionally high and further increases with the load. The architecture also simplifies the gate drive circuit through the utilization of two power switches that receive identical gate pulses. It features three inductors and four capacitors, all of small values, and incorporates WBG MOSFETs and diodes with low on-state resistance to minimize switching and conduction losses. A key advantage of this converter is its ability to achieve high voltage gain at low duty cycles. Overall, the converter's structure is simple, compact, lightweight, and offers high power density. These advantages render the proposed converter highly efficient, fitting, and dependable for RES. It operates in two distinct modes. In the first mode, at low duty ratios, inductors L_2 and L_3 operate in DCM, as illustrated in Figure. 3(a). The second mode is initiated when the load current and duty cycle increase beyond 0.6, as depicted in Figure. 3(b) and Figure. 4. In this scenario, L_3's current operates in CCM across all converter functions, while L_1's inductor current also functions in CCM at both lower and higher duty cycles. However, L_2's inductor current remains in DCM for all conditions, resonating with capacitor C_1.

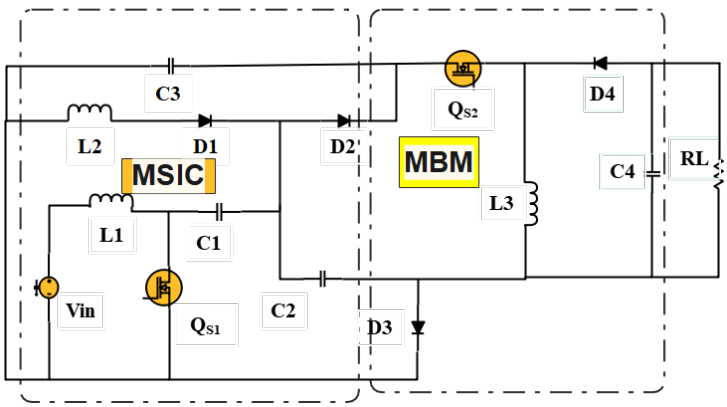


Figure 1. the Proposed of DC-DC Converter

A. Proposed Converter Operation in DCM

When the load is light with a low duty cycle, this scenario arises. During this state, the inductor L_1 operates in (CCM), whereas both L_2 and L_3 operate in (DCM). The proposed converter has the capability to operate in four different states, which are illustrated in the waveforms shown in Figure 3 (a).

Mode 1: [$_0$-t_0], both Q_{S1} and Q_{S2} are turned on, and the gate pulse drive is high, causing the two switches to be in an on state, as illustrated in Figure 2(a). The inductor L_1 charges current from the input source during this time, while L_2 is charged with current that starts from zero from C_1. C_1 is connected in series during this time as a resonant circuit between L_2 and C_1. D_1 is also connected in series with L_2 to prevent it from starting to charge current from negative values. Inductor L_3 starts charging through Q_{S2} from capacitors C_2 and C_3. C_2 and C_3 discharges its energy through L_3, while C_4, supplies energy to the load during this period. During this mode, both diodes (D_2, D_3 and D_4) are off, and D_1 is on. The voltage and current equations of the passive and power elements during this mode are shown below.

$$\begin{aligned} V_{L1} &= V_{in} \\ V_{L2} &= V_{C1} \\ V_{L3} &= V_{C2} + V_{C3} \\ V_{C4} &= V_{out} \end{aligned} \tag{1}$$

$$\left.\begin{aligned} i_{L1} &= \frac{V_{in}}{L_1} \\ i_{L2} &= \frac{Vc_1}{L_2} \\ i_{L3} &= \frac{V_{C2} + V_{C3}}{L_3} \\ I_{out} &= \frac{V_{out}}{R_L} \end{aligned}\right\}, \tag{2}$$

$$i_{L1} + i_{L2} = I_{QS1} \tag{3}$$

$$i_{L3} = I_{QS2} = I_{C2} = I_{C3} \tag{4}$$

$$i_{L2} = I_{C1} = I_{D1} \tag{5}$$

$$\begin{aligned} V_{L1} &= V_{in} - V_{C1} - V_{C2} \\ V_{L1} &= V_{in} - V_{C1} - V_{C3} \\ V_{L2} &= -V_{C2} \\ V_{L2} &= -V_{C3} \\ V_{L3} &= -V_{out} \end{aligned} \tag{6}$$

$$\begin{aligned} i_{L1} &= \frac{V_{in}}{L_1} - \frac{V_{C1}}{L_1} + \frac{V_{C2}}{L_1} \\ i_{L1} &= \frac{V_{in}}{L_1} - \frac{V_{C1}}{L_1} + \frac{V_{C3}}{L_1} \\ i_{L2} &= \frac{V_{C2} + V_{C3}}{L_2} = I_{D1} \\ i_{L3} &= \frac{V_{out}}{L_3} = I_{out} = I_{D3} \\ i_{L3} &= I_{D4} = I_{out} \\ i_{L1} + i_{L2} &= I_{C2} + I_{C3} \\ I_{C2} &= I_{C3} = I_{D2} = I_{D3} \end{aligned} \tag{7}$$

Mode 2: [t_0-t_1], both Q_{S1} and Q_{S2} are off. The gate drive pulse is low to ensure that both MOSFETs are in the off state. L_1 will discharge and transfer its energy to C_1, as well as split into two paths: one for C_2 and one for C_3. L_1 will stay in CCM because of the resonant mode between C_1 and L_2. D_1 prevents IL_1 from reaching zero at low duty cycle. Power diodes, D_2, D_3 and D_4,

are short-circuited. L_2, which has a small value, will discharge its energy to C_2 and C_3 through D_1 during the time ($\alpha 1$), as shown in Figure 3(a). Both capacitors will store a large amount of energy from L_1 and L_2. L_3 will discharge its energy to C_4, and C_4 will supply energy to the load with low output voltage ripple. The path of current for this operation mode is shown in Figure 2(b). The voltage and current equations of the passive and power elements during this mode are shown below.

Mode 3: [t_1-t_2], both Q_{S1} and Q_{S2} remain in the off state, and power diodes, D_2, D_3 and D_4, are still on. L_1 will continue to discharge energy to C_2 and C_3 through C_1, and L_2 will reach zero charge. D_1 will change from the on state to the off state during this mode. L_3's inductor current will continue to discharge energy to C_3 during time (β), and C_3 supplies power to the load. Capacitor C_2 and C_3 only charge with energy from L_1, as shown in Figure 2 (c). It can be seen that L_1 has a longer discharge time than L_2 and L_3. L_3 has a longer discharge time than L_2, and a large amount of energy supplies to the load when D_4 is in the one state. The voltage and current equations in this mode are the same as in Mode 2.

Mode 4: [t_2-t_3], in this mode, Q_{S1} and Q_{S2} are still in the off state, and only power Diode D_2 and D_3 is on. Power Diodes D_1 and D_4 are both off in this mode. C_2 and C_3 are still charging only from L_1. where, the load current (Iout) is equal to the IC_4 as shown in Figure 2(d). This method makes the suggested DC-DC converter work with a low-duty cycle during DCM, with high efficiency.

$$\left.\begin{aligned} I_{D1} &= i_{L2} = 0 \\ I_{C2} &= i_{L1} = I_{D2} \\ I_{C3} &= i_{L1} = I_{D3} \end{aligned}\right\} \tag{8}$$

Furthermore, during operation, the voltage stress on switches Q_{S1} and Q_{S2} is significantly lessened, alongside a notable reduction in their current stress. This reduction in both conduction and switching losses of the power switches contributes to a higher efficiency of the proposed converter. Additionally, the absence of pulsating input current when operating in DCM at low duty cycles enhances performance. The voltage gain of the proposed converter is determined by applying the voltage second balance principle to inductors L1, L2, and L3, as derived from equations (1) and (6).

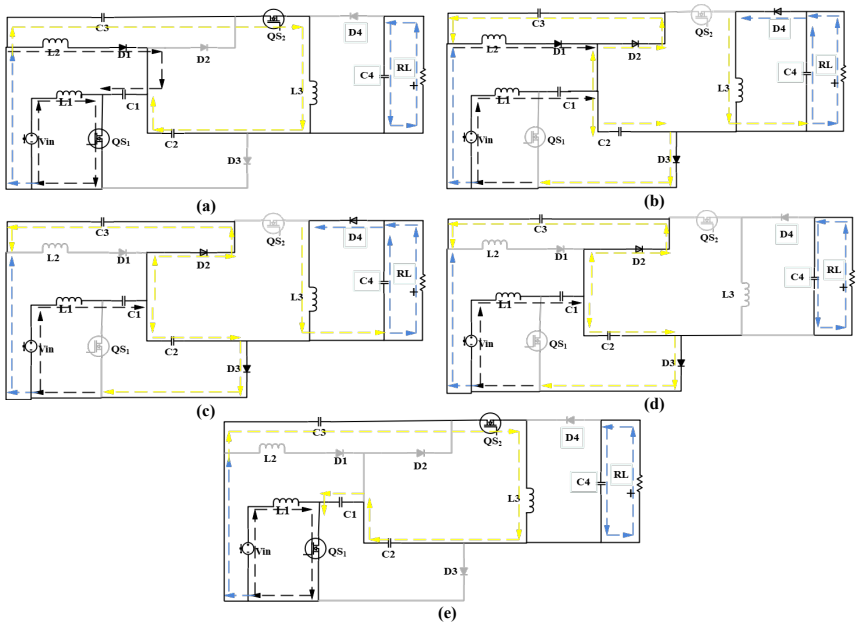


Figure 2. (a) M1 DCM, M1 CCM, (b) M2 DCM, (c) M3 DCM, M3, CCM, (d) M4 DCM, (e) M2 CCM at D1 work in ZCS, Where M is Mode.

$$\frac{1}{Ts}\left(\int_0^{DTs}(V_{in})dt+\int_D^{Ts}(V_{in}-V_{C1}-V_{C2}-V_{C3})dt+\int_{DTs}^{\alpha_1 Ts}(-V_{C2}-V_{C3})dt\right)=0 \tag{9}$$

$$\frac{1}{Ts}\left(\int_0^{DTs}(V_{C2}+V_{C3})dt+\int_{DTs}^{\beta Ts}V_{out}dt\right)=0 \tag{10}$$

After solving equation (9), the results are shown in equation (11). From Equation (12), after simplifying Equation (11), the values of α can be found in Equation (13), which is a function of the input voltage (Vin), average voltage across capacitor, and the duty cycle (D). According to equation (14), the output power (Pout) is equal to the input power (Pin) assuming ideal components, and losses are neglected. Average output current can be calculated after using the charge balance equation, the (Iout) can be obtained in equation (14). Where, the value of β of discharging time of L3 can be found in equation (15). In order to find average voltage across Q_{S2} during on and off state as in equation (16). It can be seen that average voltage across Q_{S2} is a function of (RL, L_3, and D).

$$D(V_{in}+V_{C1})+(1-D)(V_{in}-V_{C1}-V_{C2}-V_{C3})+\alpha_1(-V_{C2}-V_{C3})=0 \tag{11}$$

$$\frac{V_{C2}+V_{C3}}{V_{in}}=\frac{1}{(1+\alpha_1-D)} \tag{12}$$

$$\alpha_1=\frac{V_{in}}{V_{C2}}-1+D \tag{13}$$

$$I_{out}=\frac{(V_{C2}+V_C3)D\beta Ts}{2L_3} \tag{14}$$

$$\beta=\frac{D(V_{C2}+V_{C3})}{V_{out}} \tag{15}$$

$$V_{C2}=V_{C3}=\sqrt{\frac{{V_{out}}^2 L_3}{D^2 TsR_L}} \tag{16}$$

$$\frac{V_{out}}{V_{in}}=\frac{(V_{C2}+V_{C3})D^2TsR_L}{L_3V_{out}(1+\alpha_1-D)} \tag{17}$$

$$\frac{V_{out}}{V_{in}}=\frac{D}{(1+\alpha_1-D)}\sqrt{\frac{2}{K}}=Mdc \tag{18}$$

$$K_{crit}=\frac{(1-D)^4}{2(1+\alpha_1-D)^2} \tag{19}$$

$$K=\frac{2L_3}{TsR_L} \tag{20}$$

$$K_{crit}=\begin{cases}If\ \text{Kcrit} > \text{K The Circuit operates In DCM}\\ If\ \text{Kcrit} < \text{K The Circuit operates In CCM}\end{cases} \tag{21}$$

$$K_{crit}=\frac{(1-D)^2}{2} \tag{22}$$

Certainly, the operational efficiency and capability of the proposed converter are mathematically expressed through a series of equations that outline its performance under various conditions. The voltage gain (Mdc) of the converter is detailed in equation (17), while equation (18) delineates the Mdc as a function of a dimensionless factor, denoted as *k*. The value of *k* is derived from equation (20). Equation (19) introduces the critical value of *k* (*K*crit), which determines the operational mode of the converter—either CCM or DCM, as further expounded

in condition (21). The critical threshold for *k*, necessary to ascertain the specific operational mode of the converter, is calculated through equation (22).

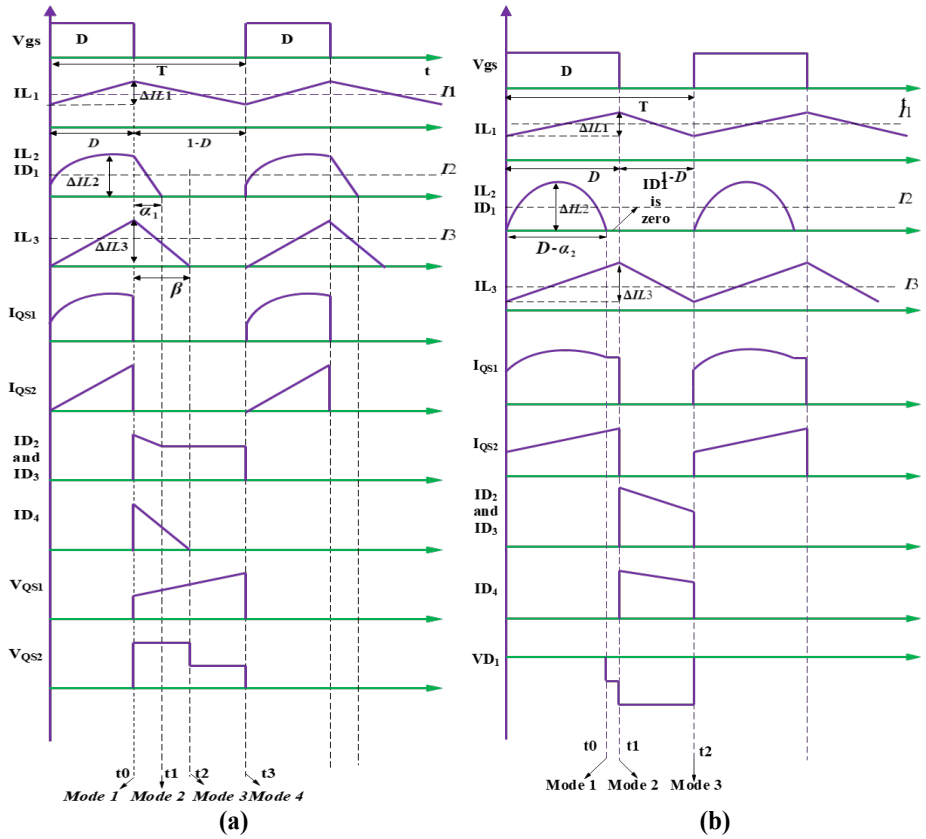


Figure 3. Voltage and Current waveforms of the Proposed converter (a) DCM (b) CCM.

B. Operation of the Converter in CCM

This mode is initiated as the load current increases, leading to a distinct operational behavior within the proposed converter. During this mode, inductors L_1 and L_3 function in CCM, indicating a steady flow of current through these components. Meanwhile, L_2 enters into resonance with capacitor C_1, and diode D_1 operates under ZCS, which minimizes switching losses and enhances efficiency. Consequently, the proposed converter showcases versatility through its ability to operate across three distinct modes. These operational modes are clearly depicted through the waveforms illustrated in Figure. 3(b), providing a comprehensive view of the converter's functionality under varying electrical loads and conditions.

Mode 1: [$_0$-t_0], both Q_{S1} and Q_{S2} are turned on, and the gate pulse drive is high, making both Mosfets in the on state. Inductor L_1 starts charging current from the input source during this period, while L_2 starts charging from the available charge in C_1, which is connected in series with L_2 during this time at resonant mode, as shown in Figure. 3 (b) of the proposed converter waveforms in CCM. Inductor L_3 starts charging through Q_{S2} two way from C_2 and C_3. The power diodes D_2, D_3 and D_4 are off state, while D_1 is in the on state during this mode, as shown in Figure. 3 (a).

Mode 2: [t_0-t_1], both Q_{S1} and Q_{S2} are still on, and power diodes D_2, D_3 and D_4 are still in the off state. Inductors L_1 and L_3 continue to charge from the input source and capacitors, respectively. C_4 is the output filter capacitor that will supply energy to the load. During this mode, L_2 will reach zero energy, and D_1 will be in the off state during this time, as shown in Figure. 2(e). This means that L_2 will be an open circuit during this period. During this time,

diodes D_2, D_3 and D_4 are still in the off state. The advantages of this method are that three diodes are in an off state and L_2 is an open circuit, which reduces losses and allows D_1 to work in ZCS and to reduce stress voltage on Q_{S1} and Q_{S2}. Overall, the efficiency of the converter will significantly increase. The voltage equations of Mode 1 and Mode 2 are shown below, and the voltage equations of L_1 and L_3 are from equation (1) and (2), respectively.

$$VL_2 = (D - \alpha_2)Vc_1 \tag{23}$$

Mode 3: [t_2-t_3] both Q_{S1} and Q_{S2} are off, and the gate drive pulse is low to enforce both MOSFETs to be in the off state as shown in Figure 2(c). L_1 and L_3 will discharge at the same time, where Capacitor C_2 and C_3 will receive energy only from L_1, and C_4 will receive energy from L_3. L_3 will discharge its energy to C_4. Furthermore, the voltage stress on power MOSFET Q_{S1} will be reduced. In addition, power diodes D_2, D_3 and D_4 will be in the on state during this time, and they will be in the off state in the next pulse.

The voltage equations are shown below. The current equations are shown below.

$$\left.\begin{aligned} V_{L1} &= V_{in} - V_{C1} - V_{C2} \\ V_{L1} &= V_{in} - V_{C1} - V_{C3} \end{aligned}\right\} \tag{24}$$

$$\left.\begin{aligned} i_{L1} &= I_{C1} = I_{C2} + I_{C3} \\ I_{D2} + I_{D3} &= i_{L1} \end{aligned}\right\} \tag{25}$$

$$\frac{1}{Ts}\left(\int_0^{DTs}(V_{in})dt + \int_D^{Ts}(V_{in} - V_{C1} - V_{C2} - V_{C3})dt + \int_{0Ts}^{D-\alpha_2 Ts}(V_{C1})dt\right) = 0 \tag{26}$$

$$\frac{1}{Ts}\left(\int_0^{DTs}(V_{C2} + V_{C3})dt + \int_{DTs}^{Ts} V_{out}dt\right) = 0 \tag{27}$$

$$\left.\begin{aligned} V_{C2} + V_{C3} &= \frac{V_{in}}{(1-D)} \\ \alpha_2 &= \frac{D(2V_{in} - V_{C2})}{(V_{in} - V_{C2})} \end{aligned}\right\} \tag{28}$$

$$V_{C2} = \frac{V_{out}(1-D)}{2D} \tag{29}$$

$$I_{QS2} = \frac{2P_{out}D}{R_L(1-D)} \tag{30}$$

$$M_{dc} = \frac{V_{out}}{V_{in}} = \frac{2D}{(1-D)^2} \tag{31}$$

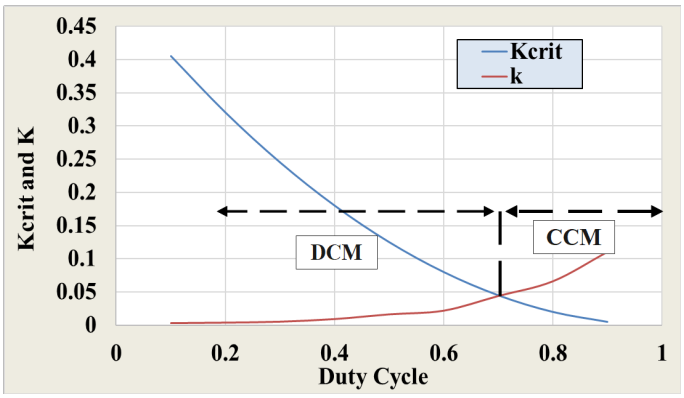


Figure 4. the proposed converter boundary condition at DCM and CCM, K and Kcrit Vs duty ratio.

Through the application of the voltage-second balance principle to inductors L_1, L_2, and L_3, and after simplifying the information from equations (1), (26), and (27), a pivotal equation emerges as equation (31). This equation details the voltage gain between the output and input in Continuous Current Mode (CCM), illustrating a significant increase in voltage gain as the load current rises, all while maintaining a zero pulsating input current. Additionally, equation (30) describes the MOSFET current within the proposed converter, and equation (29) calculates the average voltage across Q_{S2}. These equations collectively highlight the proposed converter's capability to achieve an ultra-high voltage gain, positioning it as a highly suitable option for renewable energy systems. According to Figure. 4, when the critical value of k (Kcrit) falls below the load-less factor, the converter operates in DCM. Conversely, as the load intensifies and k surpasses Kcrit, the converter transitions into CCM, as evidenced in Figure.4, particularly when the duty ratio exceeds 70%.

3. Parameter selection and design of the proposed converter

As depicted in Figure. 1, the described DC-DC converter is engineered with a minimalistic yet efficient design, featuring four capacitors and three inductors, all of which have very small values, optimizing the converter for compactness and efficiency. On the power device front, it is equipped with four diodes and two power MOSFETs, which are central to its operation. These MOSFETs are designed to switch between the on and off states seamlessly and are connected to the same pulse drive through a straightforward circuit layout, further simplifying the design and reducing complexity. The prototype of this converter has been tailored for a load capacity of 200 watts, with the capability to operate efficiently under input voltages of both 20 volts and 40 volts, details of which are methodically presented in Table 1. This setup underscores the converter's adaptability and potential for application in various power-intensive settings, highlighting its suitability for a range of operational demands.

$$L_1 \geq \frac{V_{in}D}{Fs\Delta i_{L1}} \tag{32}$$

$$L_2 = \frac{0.2R_L(1-D)}{8\pi^2 Fs V_{out} D^2} \tag{33}$$

$$L_3 = \frac{R_L(1-D)^2}{8DFs} \tag{34}$$

$$C_1 = \frac{2V_{out}D^2}{\Delta V_{C1} R_L Fs(1-D)} \tag{35}$$

$$C_2 = \frac{V_{out}D^2(3-2D)}{\Delta V_{C2} R_L Fs(1-D)^2} = C_3 \tag{36}$$

$$C_4 = \frac{V_{out}D}{\Delta V_{C4} FsR_L} \tag{37}$$

From equation (32), L_1 can be calculated as a high inductor with low ripple input current ΔiL_1. L_2 can be designed using equation (33) from the resonant equation between L_2 and C_1 after find value of C_1 from equation (35). L_3 can be obtained using equation (34), and the values of C_2, and C_3 can be found using equations (36). Filter capacitor C_4 can be calculated in equation (37) with very low ripple voltage. In the design presented in Table 1, SiC Mosfet power devices are used to verify high voltage gain with low duty cycle. The values of inductors are very small with very low internal resistance, and the Ron of the SiC power Mosfet device is only $35m\Omega$. This means that the internal resistance of passive and active elements is very small, making the proposed converter more efficient and able to operate with high performance.

Table 1. Parameters values of prototype design Of Proposed Converter

Components	Values
SiC MOSFET	AIMW120R035MIH, 40A,
SiC Schottcky	IDW40G120C5BF, 1200V,30A
L_1	200uH
L_2	7uH
L_3	100uH
C_1 C_2,C_3 C_4	2uf, 400V 100uf, 400V 220uf, 500V
V_{in}	20-40V
V_{out}	200-400V
Power	200W
Duty cycle	0.6 at 20V , 0.42 at 40V
Fs (Switching Frequency)	125kHz

4. Voltage Stress Analysis Across MOSFETs and Diode

In this analysis, we delve into the voltage stress experienced by the power MOSFETs and diodes within the proposed converter, offering a detailed calculation of these stresses and comparing the results with those of previous converter designs, as illustrated in Figure. 5. The voltage stress equations for the power MOSFETs and diodes are meticulously determined, catering to a converter that operates within an input voltage range with a minimum of 20V and a maximum of 40V. This examination not only underscores the efficiency and robustness of the proposed converter's design in handling voltage stress but also provides a comparative perspective on its performance enhancements over prior models. By assessing the voltage stresses, this section illuminates the converter's ability to maintain operational integrity and reliability under varying electrical conditions, affirming its suitability for advanced applications where such attributes are critical.

Equation (38) reveals that the Vc_1, Vc_2, and Vc_3, as well as the voltage stress on diode D_1 detailed in equation (39), are characterized by low voltage stress, indicating a design that prioritizes the longevity and reliability of these components. Equations (40) and (41) further elaborate on the VD_2 and VD_3, respectively, with the operational time period of D_1 being notably shorter than those of D_2 and D_3, as depicted in the waveforms for DCM and CCM in Figure. 3 (a) and (b). This illustrates the converter's dynamic response to varying operational modes.

Significantly, the V_{QS1} is substantially mitigated to approximately the level of the input voltage, as described in Equation (42). This reduction in stress contributes directly to the durability and efficiency of the converter. Equation (43) indicates a reduction in VD_4 when inductor L_3 operates in DCM, highlighting the converter's adaptive behavior to operational conditions to maintain optimal performance. Similarly, the stress across V_{QS2} is significantly reduced, correlating to the average voltage Vc_2 and Vc_3 during the off-state, as captured in Equation (44).

By minimizing the voltage stress on critical active elements such as diodes and switches, the proposed converter effectively reduces both conduction and switching losses. This strategic reduction in losses directly translates to an enhancement in the converter's overall efficiency, showcasing the design's effectiveness in managing operational stresses to improve performance. This feature, among others, underscores the converter's potential applicability in various scenarios, particularly where efficiency and reliability are paramount.

$$\left.\begin{aligned} V_{C1} &= \frac{V_{in}}{(1-D)} \\ V_{C2} &= \frac{V_{in}}{(1-D)} \\ V_{C3} &= \frac{V_{in}}{(1-D)} \end{aligned}\right\} \quad (38)$$

$$V_{D1} = \frac{V_{in}}{(1-D)} \quad (39)$$

$$V_{D2} = \frac{V_{in}}{2(1-D)} \quad (40)$$

$$V_{D3} = \frac{V_{in}}{2(1-D)} \quad (41)$$

$$V_{QS1} = \frac{V_{in}}{(1-D)} \quad (42)$$

$$V_{D4} = \frac{2V_{in}D}{(1-D)^2} \quad (43)$$

$$V_{QS2} = \frac{V_{in}(1+D)}{(1-D)^2} \quad (44)$$

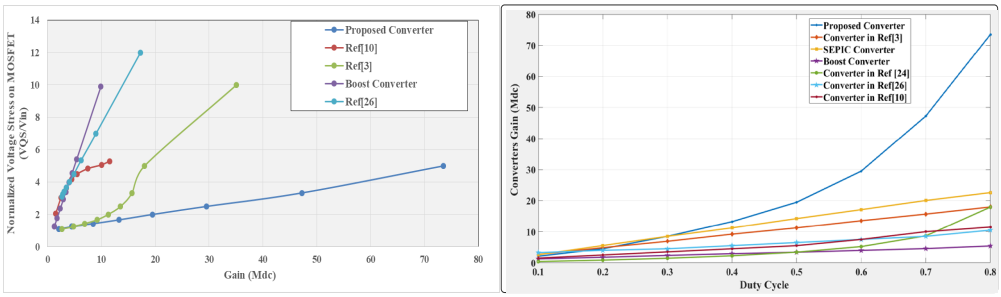
During the specific interval ($D-\alpha_2<t<D$), the voltage across diode D_1 is maintained at half of the input voltage, which facilitates the operation of D1 under ZCS conditions. This operational characteristic significantly reduces the stress on D_1, allowing it to function more efficiently and with lower losses. Concurrently, inductor L_2 is effectively rendered an open circuit during this phase, further optimizing the converter's performance by minimizing the losses associated with passive elements. Such a configuration is particularly beneficial when the proposed converter is tasked with supplying high load currents, as it ensures minimal energy wastage and enhances overall efficiency. Furthermore, the voltage stress across the switch Q_{S1} is dynamically influenced by the input voltage and the duty cycle, with the input voltage range adjustable between 20V and 40V. This adaptability ensures that both the voltage stress and current stress on Q_{S1} are significantly reduced. The resultant decrease in both conduction and switching losses underscores the proposed converter's design efficiency. By lowering these stresses, the converter not only operates more reliably but also demonstrates improved performance characteristics, making it an attractive option for systems requiring high efficiency and robust operation under varying load conditions.

5. Comparison proposed Converter with Previous work of DC DC Converter

In this section, the proposed topology is compared with previous DC-DC converters in terms of voltage stress across the MOSFET, voltage gain, and efficiency. The previous designs are simulated in MATLAB under their respective conditions. The voltage stress across the MOSFET is analyzed and verified using MATLAB for both DCM and CCM operating modes.

Figure 5 (a), illustrates a comparative analysis demonstrating that the voltage stress experienced by the power MOSFETs in the proposed DC-DC converter is significantly lower than that in both conventional boost converters and those documented in references [10, 3-26]. This analysis, facilitated by MATLAB Simulink simulations under identical conditions, highlights the proposed converter's ability to maintain low voltage stress even as DC voltage gain increases—a scenario where conventional boost converters and the models mentioned in [10, 24] show a marked increase in voltage stress on the power MOSFET devices. This characteristic not only signifies the high gain capability of the proposed converter but also indicates a reduction in switching and conduction losses of the power MOSFETs, thereby enhancing the overall efficiency of the DC-DC converter. Additionally, the proposed converter's design ensures high performance, making it particularly suitable for renewable energy

applications that demand the step-up of low DC input voltage to high DC output voltage. This requirement is met without inducing pulsating input current and while maintaining high efficiency, facilitated by the use of small-valued inductors and capacitors.



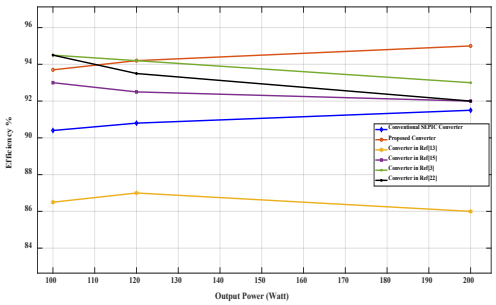


Figure 5. (a) shows the normalized voltage stress of the power MOSFET versus the voltage gain (Mdc), (b) Voltage gain (Mdc) Vs. duty cycle of converter, (c) shows the efficiency versus output power of the proposed converter and previous works.

Figure. 5 (b) showcases a voltage gain comparison between the proposed design and those from conventional and previously studied converters. This comparison reveals that the proposed converter achieves a higher voltage gain ratio than those found in [3,10,24,26] and conventional DC-DC converters, particularly noticeable at low duty cycles. Interestingly, the conventional SEPIC converter is noted to have a higher gain than the conventional Boost converter at low duty cycles, yet the proposed converter outperforms both in terms of efficiency for applications requiring high voltage gain and high power density. This makes the proposed converter an ideal candidate for energy systems where such attributes are critical for performance and sustainability.

The efficiency and performance of the proposed converter, in comparison to those documented in references [3,13,15,22] and the conventional SEPIC converter, were rigorously analyzed through simulations conducted in MATLAB Simulink, set under their respective operational conditions.

The efficiency of the proposed converter is compared with the efficiency of previous work under similar conditions, as shown in Figure 5(c). The results highlight the superior efficiency of the proposed converter, achieving an impressive 95.3% efficiency at a 200W load. This efficiency not only surpasses that of the converters referenced in [3,13,15,22] but also exceeds the performance of the conventional SEPIC converter.

A noteworthy observation from the simulations is the increase in efficiency of the proposed converter with rising load current, moving from 100W to 200W. This behavior indicates the converter's robust performance under varying load conditions and its ability to maintain high efficiency levels even as the demand on its output increases. Such a characteristic is particularly advantageous for applications where load conditions can vary widely, ensuring that the proposed

converter can deliver optimal performance without significant losses in efficiency. This attribute, combined with the high efficiency at elevated loads, positions the proposed converter as an excellent choice for applications requiring reliable, high-efficiency power conversion, such as in renewable energy systems where maximizing energy utilization is crucial.

Table 2 offers a comprehensive comparison between the proposed converter and those previously documented in references [3,10,13,15,22,24,26], highlighting several key advantages of the proposed design. Notably, the proposed converter operates at a higher switching frequency compared to other boosting converters featured in the literature. This higher switching frequency allows for the use of inductors and capacitors with much smaller values, which, in turn, leads to a more compact, lighter, and cost-effective converter design. Conversely, the converters in the aforementioned references rely on components with significantly higher values, resulting in bulkier, heavier, and more expensive solutions. Additionally, the parasitic resistance of the inductors and capacitors in these older designs is considerably higher, adversely impacting the overall efficiency of the converters.

Table 2. Proposed DC-DC Converter comparison with previous work Converters

Items	Proposed Converter	Ref[3]	Ref[10]	Ref[13]	Ref[15]	Ref[22]	Ref[24]	Ref[26]
F_{sw}(kHz)	125	40	100	45	50	66	50	5
Vin	20-40	20	50v	20	25-50v	24	24	24
Vout	200-400v	250v	400v	Out1=155vOut2=265v	200v	180	172	107v
L	3	3	3	2	1	3	3	2
C	4	3	5	8	3	3	3	3
D	4	2	3	7	4	2	3	4
Qs	2	2	1	1	2	1	1	1
Duty cycle %	42	74.2	70	77	72	88	70	45
Power (W)	200	200	200	250	198	100	100	52
Efficiency η %	95	93	92	86	94.5	94.7	91.4	91.2
Input Current Pulsation	No	No	Yes low D	Yes at low D	Yes at low D	Yes at low D	Yes at low D	Yes at low D
Mdc	$\frac{2D}{(1-D)^2}$	$\frac{(3D+1)}{(1-D)}$	$\frac{(1+2D)}{(1-D)}$	$\frac{(1+D)}{(1-D)}, Out1$ $\frac{(3)}{(1-2D)}, Out2$	$\frac{(3-2D)}{(1-2D)}$	$\frac{(2D)}{(1-D)}$	$\frac{D}{(1-D)^2}$	$\frac{(4-3D)}{(1-D)}$

Furthermore, the previous converters design typically utilize traditional power MOSFETs, which suffer from high on-state resistance (Ron), potentially diminishing the voltage gain and overall system performance. In contrast, the proposed converter achieves a low duty cycle of 60% with an input voltage of 20V and an output power of 200W, while maintaining an impressive efficiency of around 95%. This is a marked improvement over the efficiencies reported for the converters in the comparison.

The voltage gain equations further illustrate the superior voltage gain of the proposed DC-DC converter compared to those detailed in the cited references. Additionally, the converters in references [13,15] require a higher number of power diodes, and the converter in reference [13] utilizes more capacitors than the proposed design. Meanwhile, the converter in reference [24] relies on a large number of inductors and capacitors and a high duty ratio to achieve a step-up from 24V to 172V, yet it fails to offer a competitive voltage gain at high duty cycles.

In summary, the proposed converter addresses several shortcomings found in previous designs, offering an ultra-high voltage gain, minimal pulsating input current across a range of

load currents, and reduced voltage stress on MOSFETs and diodes. Its compatibility with WBG MOSFETs and a high switching frequency enables the use of smaller, low-resistance inductors and capacitors, thereby enhancing efficiency and performance. These features render the proposed converter an exemplary choice for renewable energy applications, promising high efficiency, superior performance, and high power density for a variety of application scenarios.

6. Experimental validation result and discussion

In this section, a 200W PCB prototype of the proposed converter is designed for experimental validation, as shown in Figure 6. Additionally, the proposed DC-DC converter is designed and simulated using MATLAB Simulink. The simulation and experimental results are divided into two parts: the first part when the input voltage is 40V to supply a load of 200W at a duty cycle of 0.42, and the second part when the input voltage is 20V to supply a load of 200W at a duty cycle of 0.6. Furthermore, the proposed converter can provide a variable output voltage. Furthermore, the proposed converter will undergo significant reductions in weight, size, and cost.

In Figure. 7(a), it is evident that IL_1 and IL_2 are present. Figure. 7(b) displays IL_1 and IL_3, with IL_3 operating in DCM at a load voltage of 200V. Figure. 7(c) illustrates the current through Q_{S1} and Q_{S2}, where the current through Q_{S1} equals IC_1 and IL1. Figure. 7(d) presents the load current of 1A at an output voltage of 200W and 200V. In Figure. 7(e), the load current is observed to be 0.44A at an output voltage of 200V. In terms of experimental results, the proposed converter underwent testing with variable input voltages ranging from 20V to 40V, achieving 88W for D=0.31 and 200W for D=0.42. In Figure. 7(f), the output voltage of the converter can be seen to be equal to 400V, and the current through IL_2 is observed during DCM. In Figure. 7(g) and Figure. 7(h), the input voltage and Vc_2 can be observed, where the input voltage is equal to 21V, and Vc_2 and Vc_3 are equal to 50V.

Moving to Figure. 8(a), V_{QS1} corresponds to equation (42). Figure. 8 (b) demonstrates that the average voltage across Q_{S2} during both the on and off states can be calculated using equation (16). In Figure. 8(c), VD_2 and VD_3 are displayed with low voltage stress across them. Figure. 8 (d) shows ID_2, ID_3, and ID_4, while Figure. 8 (f) depicts the current through capacitors C_1 and C_4. In Figure. 8 (e), the voltage across D_1 is half of the input voltage during this time ($D-\alpha_2<t<D$), indicating that D1 operates at low voltage stress during this period. In Figure. 8 (g) and (h), the voltage stress across L_1 and L_3 is completely eliminated, along with reduced voltage stress across inductors.

In summary, the voltage across D_1, D_2, and D_3 is reduced at high load voltage, and VQ_{S1} and VQ_{S2} are significantly reduced at high output voltage. Additionally, the system operates at DCM when supplying high load voltage and will operate at CCM when the Duty ratio is above 70%, as shown in Figure 4.

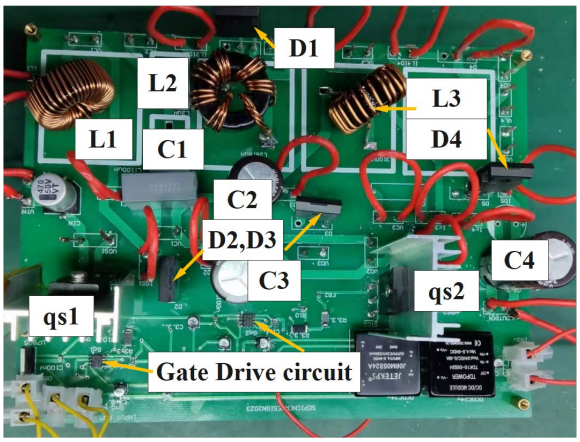


Figure 6. 200W PCB prototype of the proposed converter

7. Efficiency calculation of the Proposed Converter with Variable Input Voltage

In analyzing the efficiency of the proposed converter, especially when it operates in CCM with a 20V input voltage, it's crucial to acknowledge the non-ideal nature of its components. The inductors, capacitors, diodes, and MOSFETs within the converter are subject to parasitic resistances that can adversely affect its overall efficiency. This reality necessitates a detailed efficiency calculation that takes into account the equivalent series resistance (ESR) of these components.

For the inductors, the ESRs are denoted as rl_1, rl_2, and rl_3 for inductors L_1, L_2, and L_3, respectively. The capacitors' ESRs are represented as rc_1, rc_2, rc_3, and rc_4, corresponding to capacitors C_1, C_2, C_3, and C_4. The on-state resistance (Ron) of the power MOSFETs is a critical factor in efficiency calculations, with rds1 and rds2 specifying the on-state resistances of MOSFETs Q_{S1} and Q_{S2}. Additionally, the diodes' internal resistance (r_{D1}, r_{D2}, r_{D3}, and r_{D4}) and forward voltage (V_{FD1}, V_{FD2}, V_{FD3}, and V_{FD4}) are incorporated into the efficiency analysis to provide a comprehensive view of the converter's performance under realistic conditions.

The calculation of the converter's efficiency necessitates the determination of the root mean square current (Irms) through each component, which is a key part of equation (45). This approach allows for a nuanced understanding of how the parasitic resistances and other non-ideal component characteristics impact the converter's ability to deliver power efficiently.

A. Power Losses Calculation of Proposed converter

From Equations (45) and (46), the MOSFET RMS current during the on-state can be found, while from Equations (47), (48), and (49), all diode RMS current can be determined. From Equations (50), and (51), the inductor RMS current can be calculated. From Equations (52), (53), and (54), the capacitors' RMS current during the on and off states can be calculated.

$$I_{QS1rms} = \frac{2I_{out}\sqrt{2D-\alpha_2}}{(1-D)^2} \tag{45}$$

$$I_{QS2rms} = \frac{2I_{out}\sqrt{D^3}}{(1-D)} \tag{46}$$

$$I_{D1rms} = \frac{2I_{outD}\sqrt{D-\alpha_2}}{(1-D)^2} = iL2rms \tag{47}$$

$$\left.\begin{aligned} I_{D2rms} &= \frac{2I_{outD}}{\sqrt{(1-D)^3}} \\ I_{D3rms} &= \frac{2I_{outD}}{\sqrt{(1-D)^3}} \end{aligned}\right\} \tag{48}$$

$$I_{D4rms} = \frac{I_{out}(1+D)}{\sqrt{(1-D)}} \tag{49}$$

$$iL_{1rms} = \frac{2I_{outD}}{(1-D)^2} \tag{50}$$

$$iL_{3rms} = \frac{I_{out}}{(1-D)} \tag{51}$$

$$Ic_{1rms} = \frac{2I_{outD}}{(1-D)^2}\sqrt{D-\alpha_2} \tag{52}$$

$$Ic_{2rms} = Ic_{3rms} = \frac{I_{outD}}{\sqrt{(1-D)^3}}\sqrt{(4D(1-D)+1} \tag{53}$$

$$Ic_{4rms} = I_{out}\sqrt{\frac{D}{1-D}} \tag{54}$$

A. Conduction Losses Calculation of Mosfet Devices

The conduction power losses of the power MOSFETs in the proposed converter can be found using equation (55), where P_{codL1} is the conduction power loss in Q_{S1} and P_{codL2} is the conduction power loss in Q_{S2}.

$$P_{codL1} = \frac{4P_{out}(2D-\alpha_2)}{RL(1-D)^4} rds_1$$
$$P_{codL2} = \frac{4P_{out}D^3}{RL(1-D)^2} rds_2 \quad (55)$$

A.1. Switching Losses calculation of MOSFETs Devices

$$P_{SWL} = V_{QS}{}^2 FsCo$$
$$P_{SWL1} = \frac{FsV_{in}{}^2 Co_1}{2(1-D)^2} \quad (56)$$
$$P_{SWL2} = FsCo_2 \frac{V_{in}{}^2(1+D)^2}{2(1-D)^4}$$

Switching power losses in Q_{S1} and Q_{S2} can be found from Equation (56), where Co_1 and Co_2 are the output capacitors of the power MOSFET and are equal. PswL refers to the power switching losses of the MOSFET.

A.2. Total power loss in Mosfet devices

$$P_{LM1,2} = \frac{4P_{out}(2D-\alpha_2)rds1}{RL(1-D)^4} + \frac{4P_{out}D^3 rds2}{RL(1-D)^2} + \frac{FsV_{in}{}^2 Co_1}{2(1-D)^2} + \frac{V_{in}{}^2(1+D)^2 FsCo_2}{2(1-D)^4} \quad (57)$$

Equation (57) considers $P_{LM1,2}$ as the total power dissipation in power MOSFETs Q_{S1} and Q_{S2} of the proposed converter.

A.3. Diode Power Losses

$$\left.\begin{aligned} PDr &= IDrmsrd \\ PDr1 &= \frac{4PoutD^2(D-\alpha_2)}{RL(1-D)^4} rd1 \\ PDr2 &= \frac{4PoutD^2}{RL(1-D)^3} rd2 \\ PDr3 &= \frac{4PoutD^2}{RL(1-D)^3} rd3 \\ PDr4 &= \frac{Pout}{RL(1-D)^2} rd4 \end{aligned}\right\} \quad (58)$$

$$\left.\begin{aligned} I_{D1ava} &= \frac{2I_{out}D(D-\alpha_2)}{(1-D)^2} \\ I_{D2ava} &= \frac{2I_{out}D}{(1-D)} \\ I_{D3ava} &= \frac{2I_{out}D}{(1-D)} \\ I_{D4ava} &= I_{out} \end{aligned}\right\} \quad (59)$$

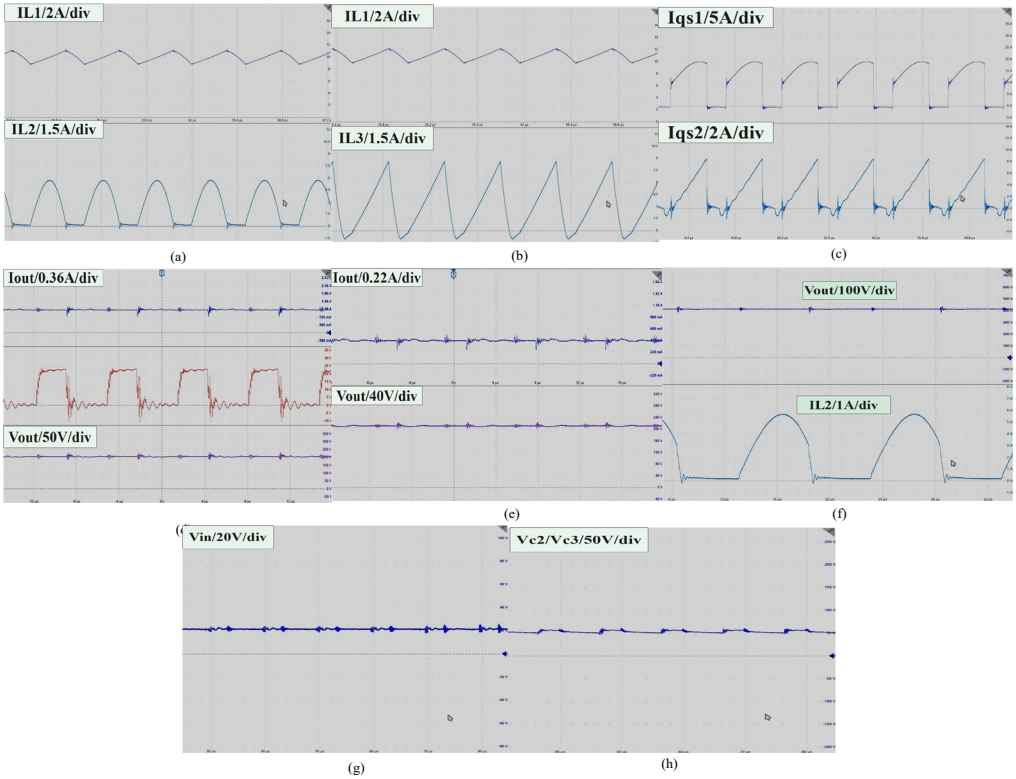


Figure 7. (a) IL_1, IL_2 (b) IL_1, IL_3, and Vo=200v (c), Current through Q_{s1} and Q_{S2} (d) Load current 1A at 200v output voltage 200w (e) load current 0.44A at load voltage 200v at Vin=40 at D=0.31(f) Vo=400v and IL2 (g) input voltage,Vin=21 (h) Vc2 and Vc3 at Vin=21 at D=0.6 at 200W.

$$\left.\begin{aligned} P_{DVFD} &= I_{Dava} V_{FD} \\ P_{DVFD1} &= V_{FD1}\frac{2I_{out}D(D-\alpha_2)}{(1-D)^2} \\ P_{DVFD2} &= V_{FD2}\frac{2I_{outD}}{(1-D)} \\ P_{DVFD3} &= V_{FD3}\frac{2I_{outD}}{(1-D)} \\ P_{DVFD4} &= V_{FD4} I_{out} \end{aligned}\right\} \tag{60}$$

From equation (58), PDr is the power loss in the diode due to the internal resistance of the diodes, which is obtained by multiplying IDrms by the internal resistance of the diode (rd). From equation (60), P_{DVFD} represents the diode power losses due to the forward voltage in the diodes. Equation (59) gives the average current through the diode.

$$P_{DL1,2,3,4} = P_{Dr1,2,3,4} + P_{DVFD1,2,3,4} \tag{61}$$

From equation (61) can be found P_{DL} total power losses in all diodes due to internal resistance of diode and forward voltage.

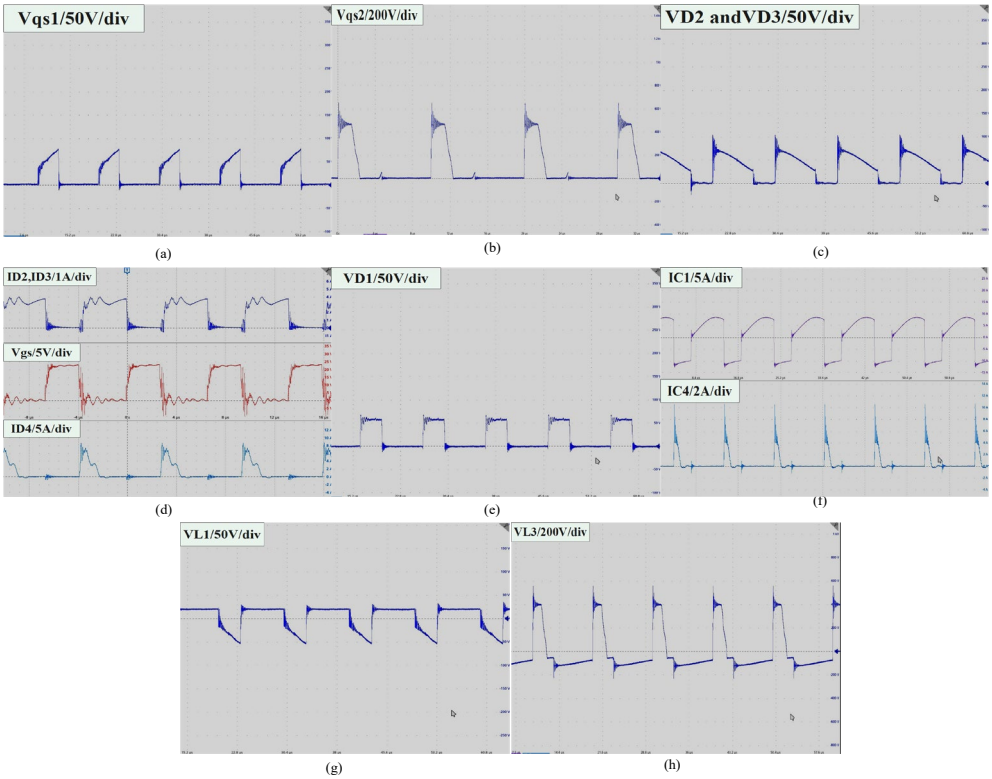


Figure 8. (a) VQs_1 (b) VQs_2 (c) VD_2 and VD_3 (d) ID_2,ID_3 and ID_4 (e) VD1(f) IC_1 and IC_4 (g) VL_1 (h)VL_3

A.5 Power Losses in Inductors

$$P_{LL} = iLrms^2 rl \tag{62}$$

$$P_{LL1} = \frac{4P_{out}D^2}{RL(1-D)^4} rl1$$

$$P_{LL2} = \frac{4P_{out}D^2(D-\alpha_2)}{RL(1-D)^4} rl2$$

$$P_{LL3} = \frac{4D^2P_{out}}{RL(1-D)^2} rl3$$

From equation (62), can be obtained P_{LL} power losses in all inductors and by adding power losses of three inductors, can be got total power losses in all inductors.

A.6 Power Losses in Capacitors

$$P_{CL} = Icrms^2 rc1 \tag{63}$$

$$P_{CL1} = \frac{4PoutD^2(D-\alpha_2)}{RL(1-D)^4} rc1$$

$$P_{CL2} = P_{CL3} = \frac{PoutD^2(4D(1-D)+1)}{(1-D)^3} rc2$$

$$P_{CL4} = \frac{PoutD}{RL(1-D)} rc4$$

Power losses in all capacitors can be obtained from Equation (63). By adding the power losses of the three capacitors, the total power losses in all capacitors can be calculated.

A.7 Proposed Converter Power losses

$$T_{PL} = P_{LM1,2} + P_{DL1,2,3,4} + P_{LL1,2,3} + P_{CL1,2,3,4} \tag{64}$$

$$\eta = \frac{P_{out}}{P_{out} + TPL} 100\% \tag{65}$$

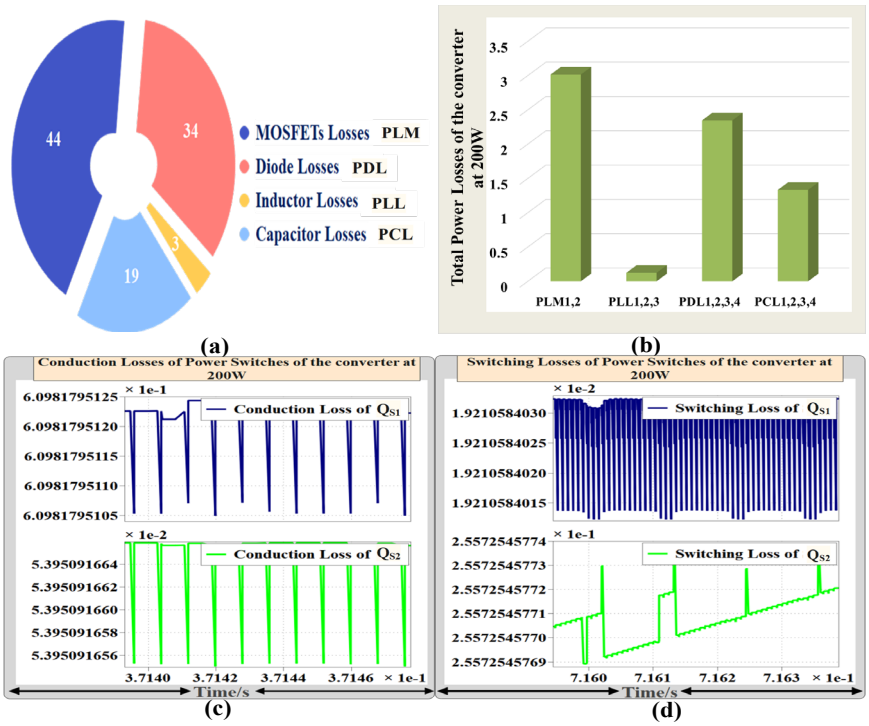


Figure 9. (a) percentage losses of each components in the Proposed Converter (b) Total power losses of the system at 200W, (c) condution losses of the power MOSFETs at 200W (d), switching losses of the power switches in the converter.

Equation (64) outlines how to determine the total power losses (T_{PL}) in the proposed converter, including losses from MOSFETs, diodes, inductors, and capacitors. Equation (65) explains how to calculate its efficiency. To reduce conduction losses, it is advised to choose power MOSFETs with minimal resistance and diodes that have low forward voltage and internal resistance. The inductor should be capable of handling high switching frequencies and possess low internal resistance, with flat wire inductors being used in this case for their low resistance and suitability for high frequencies.

In Figure. 9(a), it's depicted that the inductors' loss in the proposed converter at a 200W power setting is approximately 3% of the total losses. Figure. 9(b) indicates that at a 40V input voltage, the converter experiences losses of 6.8W. Additionally, Figure. 9(c) and Figure.9 (d) detail the conductive and switching losses for the power switch, showing that Sw1's conductive losses amount to 0.6W, and its switching losses to 0.019W. It is also noted that operating the converter under conditions of low duty cycles, high loads, and maximum input voltage greatly diminishes losses, positioning this converter as highly efficient for scenarios requiring stable high output voltages amid variable loads and input voltages.

From Figure. 10, the efficiency of this DC-DC converter is documented at 95.3% when operating at duty cycles greater than 0.6 and with an input voltage of 40V. The efficiency shows an increase with duty cycles starting from 0.3 upwards, suggesting that the converter has a broad range of flexibility in stepping up from low to high output voltages by adjusting duty cycles. Moreover, an increase in input voltage allows for a reduction in duty cycle to maintain the desired output voltage. This converter is demonstrated to efficiently manage from light to heavy loads, as evidenced in Figure. 10.

From Figure 10, it can see that the efficiency of proposed converter when Vin =20 at 200W is 93.5%. While the efficiency of the converter is 95.3% when input voltage increased from 20V to 40V. In addition, when input voltage increase, the proposed converter can supply high load with low duty cycle. That means, the proposed converter has high efficiency when input voltage increased and can work at low duty cycle. Furthermore, low duty ratio this means, low conduction and switching losses, high efficiency, low voltage stress on power devices, draw low input current with no pulsating, using power devices with low internal resistance.

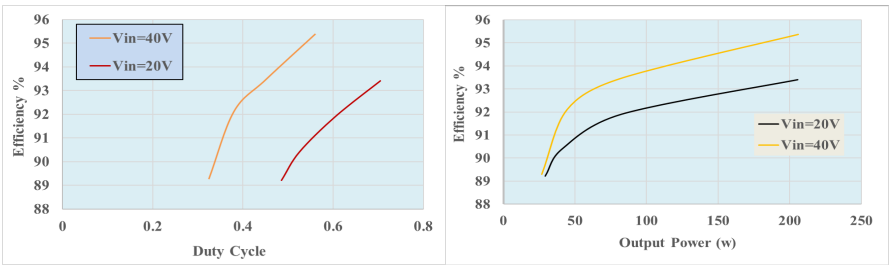


Figure 10. (a) Efficiency of Proposed Converter Vs. duty cycle, (b) Efficiency of Proposed Converter Vs. Output Power (W)

8. Conclusion

As a result, a high voltage gain DC-DC converter specifically designed for renewable energy systems is proposed, combining the MSIC with the MBM. The MSIC incorporates a diode in series with the inductor, achieving significant voltage gain while effectively mitigating pulsating input current at low duty cycles. The interleaved MSIC with a main switch manages current through the main circuit, reducing conduction losses and increasing efficiency. Additionally, the diode in the MSIC operates with Zero Current Switching , minimizing voltage stress across it. Furthermore, adding MBM to the proposed topology verifies high voltage gain at low duty cycles. The components of the MBM operate under low voltage and current stress, which enhances system efficiency and significantly reduces total power loss.

The proposed topology operates at high switching frequencies, showcasing superior efficiency while minimizing switching and conduction losses. Its compact size and lighter weight distinguish it from previous non-isolated DC-DC converters, which typically require a higher count of diodes and switches. Comparative analysis with existing studies and standard DC-DC converters underscores its considerable advantages in voltage gain and efficiency. Specifically, the converter achieves an impressive efficiency of 95.5% at 200W with a 20V input voltage and a duty cycle of 0.6, and maintains 95.3% efficiency at the same power level with a 40V input voltage. Its efficiency further increases with the load current, demonstrating versatility across a range of applications. The converter's duty cycle flexibility ensures efficient high-power delivery and the elevation of low input voltage to high output voltage, meeting diverse energy demands. Crucially, this design minimizes voltage stress on power devices, eliminates input current pulsation across a broad spectrum of duty cycles, and leverages SiC MOSFETs with low R on for heightened efficiency and thermal robustness. By reducing the values of components and the size of the circuit through the adoption of high switching frequencies, the proposed converter marks a significant step forward in enhancing the performance and efficiency of renewable energy systems.

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